

EdTech Platform in Semiconductor Space to Democratize Chip Design and
Development Ecosystem for Masses

Day wise plan of the bootcamp

Day	Focus area	Topics to be covered
Day 1 Verilog Fundamentals & Tool Flow	RTL Basics + Linux	• Fundamentals of Verilog: syntax, modules, hierarchy • Behavioural vs Structural modelling • Linux & VI command lab Hands-on Labs: • AND gate in Verilog • 4-bit counter • Ripple up counter • Verilator: 4×1 MUX • Verilator: Half Adder
Day 2 Synthesis & IP Design Basics	Synthesizable RTL + IP Flow	• Synthesizable vs Non-synthesizable constructs • Common RTL coding mistakes • Introduction to Yosys (RTL → Gate) • Synth vs Non-synth examples (practical comparison) Hands-on Labs: • JK Flip-Flop (synth-safe RTL) • Synth vs non-synth RTL demo • IP design methodology: Specification → RTL → Verification • UART RX (simple RTL)
Day 3 Bus Interfaces, CDC & Clocking	IP Integration+ Timing	• IP integration at subsystem level • Signal interfacing basics • Bus protocols overview (APB focus) • APB-UART integration

		CDC & Reset Concepts: • Metastability (without synchronizer) • Fixing metastability using 2-stage synchronizer • CDC & RDC handling basics • Introduction to SoC clocking & reset architectures • Reset types (sync/async)
Day 4 Low Power, Multi-Clock & Reset Design	Advanced RTL Techniques	• Multi-clock domain architectures • Clock multiplexers & dividers • Multi-stage synchronizers for stable CDC • FIFO design for asynchronous interfaces Low Power Design: • Clock gating concepts & RTL coding • Power gating introduction • UPF low-power basics • Low-power Verilog coding exercises • Reset architecture: global & local resets • Reset synchronization logic
Day 5 Mini-SoC Project & Debugging	Integration + Industry Practice	• Designing simple IPs: UART, GPIO, Timer • Writing bus interfaces (APB / AHB-Lite basics) • Inserting clock/reset synchronization logic • Integrating multiple IPs into a mini-SoC Project & Collaboration: • Mini-SoC project using GitHub • Team-based collaboration using GIT • Debugging SoC integration – detecting a real bug • Introduction to assertions for CDC/RDC checking