# SCHEME OF INSTRUCTION AND SYLLABI

## Master of Engineering

**A TWO YEAR (I – IV Semesters) PG Program**

**in**

**EMBEDDED SYSTEMS & VLSI DESIGN**

**R-26 Curriculum (with effect from AY 2026-27)**


## CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY

(Autonomous Institution under UGC, Affiliated to Osmania University)

Department of Electronics and Communication Engineering

Accredited by NBA and NAAC-UGC

Chaitanya Bharathi (Post), Gandipet, Hyderabad–500075

**CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)**

***OUR MOTTO: SWAYAM TEJASWIN BHAVA***

## VISION and MISSION of the INSTITUTE

### Vision

To be a centre of excellence in technical education and research.

### Mission

To address the emerging needs through quality technical education and advanced research.

## VISION and MISSION of the DEPT. of ECE

### Vision

To emerge as a vibrant model of excellence in education, research and innovation in Electronics and Communication Engineering.

### Mission

M1: To impart strong theoretical and practical knowledge of the state of art technologies to meet growing challenges in the industry.

M2: To carry out the advanced and need based research in consultation with the renowned research and industrial organizations.

M3: To create entrepreneurship environment including innovation, incubation and encourage to patent the work.

## DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

### Program Educational Objectives of ME (Embedded Systems and VLSI Design) Program

| | |
|---|---|
| PEO1 | Graduates will apply engineering expertise to solve real world problems in the areas of Embedded Systems and VLSI Design. |
| PEO2 | Graduates will have the ability to adopt latest technologies. |
| PEO3 | Graduates will be able to carry out research in the fields of Micro Electronics and Embedded Systems. |
| PEO4 | Graduates will develop professional ethics, effective communication skills, self-confidence and societal responsibilities. |

### Program Outcomes of ME (Embedded Systems and VLSI Design) Program

| | |
|---|---|
| PO1 | An ability to independently carry out research /investigation and development work to solve practical problems. |
| PO2 | An ability to write and present a substantial technical report/document. |
| PO3 | Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program. |
| PO4 | Students will be able to use modern engineering tools/software to design and develop Embedded and VLSI Systems as per the needs of the Industry. |
| PO5 | Students will be able to develop self-confidence, team work, skills for lifelong learning and committed to social responsibilities. |

**CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)**

## R-26 Curriculum (with effect from AY 2026-27)

**M.E (Embedded Systems & VLSI Design)**

**SEMESTER – I**

| S.no | Course Code | Title of the Course | Scheme of Instruction | | | Scheme of Examination | | | Credits |
|---|---|---|---|---|---|---|---|---|---|
| | | | Hours per week | | | Duration of SEE in Hours | Maximum Marks | | |
| | | | L | T | P/D | | CIE | SEE | |
| **THEORY** | | | | | | | | | |
| 1 | 26ECC201 | Analog and Digital CMOS VLSI Design | 3 | -- | -- | 3 | 40 | 60 | 3 |
| 2 | 26ECC202 | Advanced Microcontrollers and programmable DSP | 3 | -- | -- | 3 | 40 | 60 | 3 |
| 3 | | Program Elective-I | 3 | -- | -- | 3 | 40 | 60 | 3 |
| 4 | | Program Elective-II | 3 | -- | -- | 3 | 40 | 60 | 3 |
| 5 | 26MEM101 | Research Methodology and IPR | 2 | -- | -- | 3 | 40 | 60 | 2 |
| 6 | | Audit Course-I | 2 | -- | -- | 2 | -- | 50 | Non-Credit |
| **PRACTICALS** | | | | | | | | | |
| 7 | 26ECC203 | Analog CMOS VLSI Design Lab | -- | -- | 2 | -- | 50 | -- | 1 |
| 8 | 26ECC204 | Digital CMOS VLSI Design Lab | -- | -- | 2 | -- | 50 | | 1 |
| 9 | 26ECC205 | Microcontrollers and programmable DSP Lab | -- | -- | 2 | -- | 50 | -- | 1 |
| 10 | 26ECC214 | AI Workshop for ES and VLSI Design | -- | -- | 2 | -- | 50 | -- | 1 |
| **Total** | | | **16** | **--** | **8** | **17** | **400** | **350** | **18** |
| **Clock Hours Per Week: 24** | | | | | | | | | |

**L: Lecture** **D: Drawing** **CIE: Continuous Internal Evaluation**

**T: Tutorial** **P: Practical/Mini Project /Dissertation** **SEE: Semester End Examination**

**26ECC201**

## ANALOG AND DIGITAL CMOS VLSI DESIGN

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Analog and Digital design concepts.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Educate about the different Models of MOSFET, so that it can be used in analytical analysis and modelling of the circuits.
2. Demonstrate the construction, analysis and design of basic circuits of Analog IC Design.
3. Demonstrate the construction, analysis and design of basic circuits of Digital IC Design.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Choose and apply appropriate MOS model for analytical modelling/analysis of the circuits.
2. Choose appropriate amplifier or current mirror circuit for a given application or specification.
3. Design various types of amplifiers, Op-Amps and current sources as per the required specifications.
4. Design and analyze any combinational circuits for a given application.
5. Design and analyze sequential circuits for any given application.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 3 | 3 |
| **CO2** | 3 | 2 | 3 | 3 | 3 |
| **CO3** | 3 | 2 | 3 | 3 | 3 |
| **CO4** | 3 | 2 | 3 | 3 | 3 |
| **CO5** | 3 | 2 | 3 | 3 | 3 |

**UNIT – I**

**MOS Modelling:** Basic MOS Device Physics, MOS structure, MOS I/V Characteristics: Threshold Voltage, Band-Bending, Derivation of I/V Characteristics, Second Order Effects, MOS Device Layout, MOS Device Capacitances, MOS Low Frequencies Small Signal Models, Long Channel vs Short Channel, Short channel effects, Latch-up.

**Single Stage Amplifiers:** Basic Concepts, Common Source Stage- with Resistive Load, Current Source Load, Triode Load, with Source Degeneration, Source Follower, Common Gate Stage, Cascode Stage, Folded Cascode.

**UNIT – II**

**Current Mirrors:** Basic Current Mirrors, Cascode Current Mirrors, Wide-Swing Current Mirrors, Wilson and Wildar Current Mirrors.

Frequency Response of Single Stage Amplifiers, Miller Effect, Association of Nodes with Poles, **Frequency Response of Single Stage Amplifiers:** CS Stage, Source Follower, Common Gate Stage, Cascode Amplifier.

**Noise:** Sources and Types of Noise in MOSFET - Flicker Noise and Thermal Noise, Representation of Noise in Circuits.

**UNIT – III**

**Differential Amplifiers:** Single Ended vs Differential Amplifiers, Basic Differential Pair, Small signal and large signal analysis of Basic Differential Pair, Common Mode Response, Differential Pair with MOS Load. Frequency Response of Differential Amplifier.

**Operational Amplifiers:** One Stage Op-Amp, Two Stage Op-Amp, Gain Boosting, Common Mode Feed-Back, Input Range Limitations, Slew Rate, PSRR.

**Stability and Frequency Compensation**: General Considerations, Multi-Pole System, Phase Margin, Frequency Compensation, Compensation of Two Stage Op-Amp, Compensation Techniques. Typical Design Procedure for 2-Stage Op-Amp.

**UNIT – IV**

**CMOS-Inverter:** MOS Static Behavior,

**Inverter:** Static CMOS Inverter, Switching Threshold and Noise Margin Concepts and Their Evaluation of Dynamic Behavior, Power Consumption, Static and Dynamic Analysis of CMOS inverter, Cascading of CMOS gates, Fanout, delay, ESD Protection-Human Body Model.

**UNIT – V**

**Combinational Logic:** Static CMOS Design, Logic Effort, Ratioed Logic, Pass Transistor Logic, Dynamic Logic, Speed and Power Dissipation in Dynamic Logic, Cascading Dynamic Gates, CMOS Transmission Gate Logic.

**Sequential Logic:** Static Latches and Registers, MUX Based Latches, Static SR Flip-Flops, Master-Slave Edge- Triggered Register, setup and hold time, Dynamic Latches, and Registers.

**TEXT BOOKS:**

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill. 2002.
2. J P Rabaey, A P Chandrakasan, B Nikolic, “Digital Integrated circuits: A design perspective”, Prentice Hall electronics and VLSI series, 2nd edition 2003.
3. Kang, S. and Leblebici, Y., “CMOS Digital Integrated Circuits, Analysis and Design”, TMH, 3rdEdition 2003.

**SUGGESTED READING:**

1. David Johns, Ken Martin, “Analog Integrated Circuit Design”, John Wiley & sons. 2004.
2. Jacob Baker.R.et.al., “CMOS Circuit Design”, IEEE Press, Prentice Hall, India, 2000.
3. Paul. R. Gray & Robert G. Major, “Analysis and Design of Analog Integrated Circuits”, John Wiley & sons. 2004.

**26ECC202**

## ADVANCED MICROCONTROLLERS AND PROGRAMMABLE DSP

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Microprocessors and Interfacing, Digital Signal Processing fundamentals, Programming in C.

**COURSE OBJECTIVES:**

**This course aims to:**

1. To understand ARM Cortex-M architecture, programming model.
2. To develop embedded applications using C/assembly with efficient peripheral interfacing.
3. To introduce DSP architecture and implement basic signal processing algorithms for real-time applications.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Compare and select ARM processor core based on requirements of embedded application.
2. Analyse various features of ARM Cortex-M4 Series processor.
3. Develop the skills to program ARM Cortex-M4 processors.
4. Design interfacing applications on ARM Cortex-M4 based microcontroller.
5. Apply various signal processing applications on DSP processor based platforms.

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 1 | 1 | 1 |
| **CO2** | 3 | 2 | 2 | 3 | 2 |
| **CO3** | 2 | 2 | 3 | 3 | 1 |
| **CO4** | 3 | 2 | 2 | 3 | 2 |
| **CO5** | 2 | 2 | 3 | 3 | 3 |

**UNIT - I**

**Background of ARM & ARM Cortex-M Architecture:** Evolution of ARM architecture, Cortex-M series overview, Cortex-M4 architecture: pipeline, registers, memory organization, Programming model: stack, modes, exceptions and interrupts, Memory model and data types, Introduction to CMSIS (Cortex Microcontroller Software Interface Standard)

**UNIT - II**

**ARM Programming (Assembly & Embedded C):** Instruction set overview (Thumb/Thumb-2 basics), Data processing, branching, and memory access instructions, Assembly programming fundamentals, Embedded C programming for Cortex-M, Mixed C and assembly programming, Debugging and development tools.

**UNIT - III**

**Cortex-M4 Peripherals:** Nested Vectored Interrupt Controller (NVIC), System Control block, System timer- SysTick, Memory protection unit (MPU), Floating point unit (FPU).

**UNIT - IV**

**Cortex- M4 Microcontroller:** Tiva C Series TM4C123G ARM Cortex M4 Microcontroller Features, Specifications. Clock system, PLL, and power modes (sleep/deep sleep). Peripheral interfacing: GPIO, timers, ADC with sensors, PWM for control applications. Overview and programming of serial communication protocols –UART, SSI, I2C.

**UNIT - V**

**TMS320C67XX:** Features of C67XX Processors, Internal Architecture, Functional units and operation, Data paths, Cross paths, Control Register File, Addressing modes, Overview of Fixed and Floating point Instructions, Conditional Operations, Parallel Operations. Implementation of DSP algorithms such as convolution, FIR and IIR filters using C.

**Application Development Tools:** Code composer studio (CCS), Basic concepts of real-time signal processing.

**TEXT BOOKS:**

1. Joseph Yiu, "System-on-Chip Design with ARM Cortex-M Processors", Arm Education, Latest Edition.
2. Jonathan W. Valvano, "Embedded Systems: Real-Time Interfacing to ARM Cortex-M Microcontrollers", Latest Edition (2024).
3. Cem Ünsalan et al., "Embedded Machine Learning with Microcontrollers", Springer, 2025.

**SUGGESTED READING:**

1. Trevor Martin, "The Insider's Guide to ARM Cortex-M Development", Packt, 2023.
2. ARM Education, "Digital Signal Processing using ARM Cortex-M Microcontrollers", ARM Publications.
3. ARM University Program, "Fundamentals of SoC Design on ARM Cortex-M Microcontrollers", 2023 Edition.
4. Texas Instruments, TMS320C67x/C67x+ DSP CPU and Instruction Set Reference Guide (Latest available).

**26ECE201**

**LOW POWER VLSI DESIGN**
**(Program Elective - I)**

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Analog and Digital CMOS VLSI Design.

**COURSE OBJECTIVES**:
**This course aims to:**

1. To develop a strong understanding of power dissipation mechanisms in CMOS circuits and explore techniques to minimize power at device and circuit levels.
2. To enable students to design and analyze low-power digital circuits, including clock networks, arithmetic units, and memory subsystems.
3. To provide knowledge of system-level and architectural approaches for power optimization in modern VLSI and microprocessor-based systems.

**COURSE OUTCOMES:**
**After completion of this course, students will be able to:**

1. Analyze sources of power dissipation and the impact of technology scaling, Vdd, and Vt in CMOS circuits.
2. Apply device- and circuit-level techniques such as transistor sizing, and low-power FF design.
3. Evaluate and design low-power clock distribution networks and interconnect strategies.
4. Design and optimize low-power logic circuits and memory subsystems using appropriate techniques.
5. Analyze and apply system-level and architectural power optimization techniques in microprocessor-based systems.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 1 | 2 | 2 | 1 | 1 |
| **CO2** | 1 | 2 | 3 | 1 | 1 |
| **CO3** | 1 | 3 | 3 | 1 | 1 |
| **CO4** | 2 | 3 | 3 | 1 | 2 |
| **CO5** | 2 | 3 | 3 | 2 | 2 |

**UNIT – I**
**Fundamentals of Power Dissipation in CMOS:**
Introduction to low-power design; sources of power dissipation in digital CMOS circuits (dynamic, short-circuit, and leakage power); analysis of switching activity; dynamic power dissipation in CMOS; impact of supply voltage (Vdd) and threshold voltage (Vt) on power and speed; constraints in threshold voltage scaling; overview of technology scaling and its impact on power; and emerging low-power design methodologies.

**UNIT – II**
**Device and Circuit Level Low-Power Design:**
Design degrees of freedom for low-power optimization; transistor sizing techniques; optimization of gate oxide thickness; power consumption in combinational and sequential circuits; low-power design of flip-flops and latches; impact of high-capacitance nodes; energy recovery and charge recycling techniques; and high-performance low-power circuit styles.

**UNIT – III**

**Low-Power Clocking and Interconnect Design:**

Power dissipation in clock distribution networks; analysis of clock loading and switching; single driver versus distributed buffering techniques; buffer sizing under process variations; skew optimization (zero skew vs tolerable skew); low-power clocking strategies; and chip–package co-design for efficient clock and interconnect power reduction.

**UNIT – IV**

**Logic-Level Optimization and Memory Design:**

Power estimation techniques at logic level; power minimization strategies during synthesis; low-power design of arithmetic components (adders and multipliers) using different circuit styles; memory subsystem power analysis; sources of power dissipation in SRAM and DRAM; and techniques for reducing memory power consumption.

**UNIT – V**

**System-Level and Architectural Low-Power Design:**

Power management techniques in microprocessors; architectural trade-offs for low-power design; voltage scaling and selection of supply voltage; system-level clocking strategies; implementation challenges in low-power systems.

**TEXT BOOKS:**

1. A.P. Chandrakasan and R.W. Brodersen, *"Low Power Digital CMOS Design"*, Springer, 2012.
2. Jan M. Rabaey and Massoud Pedram, *"Low Power Design Methodologies"*, Kluwer Academic Publishers, 1996
3. Kaushik Roy and Sharat Prasad, *"Low Power CMOS VLSI Circuit Design"*, John Wiley & Sons, 2009 (Wiley India Edition).

**SUGGESTED READING:**

1. Gary Yeap, *"Practical Low Power Digital VLSI Design"*, Kluwer Academic Publishers, 1998
2. Ajit Pal, *"Low-Power VLSI Circuits and Systems"*, Springer, 2015.

**26ECE202**

## CPLD AND FPGA ARCHITECTURES

(Program Elective - I)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Digital Design using Multiplexers and Look-up tables.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Study various Reconfigurable computing systems Architectures and its features.
2. Understand the different programming technologies, PAR, and testing.
3. Study the design flow and tools for FPGA and ASICs.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Describe the concepts of Reconfigurable computing systems and able to implement logic functions using them.
2. Analyze the various architectures of CPLD and FPGA.
3. Summarize the various features of advanced FPGAs.
4. Understand the concepts of placement and routing algorithms.
5. Demonstrate VLSI tool flow for FPGA and ASICs and relate the testing concepts

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 1 | 1 | 1 | 1 |
| **CO2** | 3 | 1 | 1 | 1 | 1 |
| **CO3** | 3 | 1 | 1 | 2 | 1 |
| **CO4** | 2 | 1 | 1 | 1 | 1 |
| **CO5** | 3 | 1 | 1 | 2 | 1 |

**UNIT – I**

**Programmable Logic Devices:**

Introduction, Evolution: Programmable Read only Memory (PROM), Programmable Logic Array (PLA) and Programmable Array Logic (PAL), Implementation with PLDs, Introduction to CPLD, FPGA and ASIC, Programming Technologies: SRAM, Anti Fuse, EEPROM and Flash Memory.

**UNIT – II**

**CPLD: Complex Programmable Logic Devices**:

Architecture and Features of Altera Max 7000 Series CPLD, AMD Mach 4 and Xilinx 9500 Series. FPGAs: Field Programmable Gate Arrays: Logic Blocks, Routing Architecture and Features of Xilinx XC4000, Spartan II, Virtex II and Actel Act1, Act2, Act3 FPGAs.

**UNIT – III**

**Advance FPGAs:**

Architectures and Features of Xilinx Spartan- 7 Boolean board, Virtex-6, and Alteras Startix FPGAs. Introduction to Xilinx Zynq Board.

**UNIT – IV**

**Placement: Objectives, Placement Algorithms:**

Min-Cut-Based Placement, Iterative Improvement Placement, Simulated Annealing. Routing: Objectives, Segmented Channel Routing, Maze Routing, Routability Estimation, Computing Signal Delay in RC Tree Networks.

**UNIT – V**

**Design Flow and Testing:**

Design Flow for FPGA and ASIC, Digital Front End and Back-End Tools For FPGAs And ASICs, Verification: Introduction, Logic Simulation, Design Validation, Timing Verification, Testing. Concepts: Failures, Mechanisms and Faults, Fault Coverage, ATPG, BIST Methods and Programmability Failures.

**TEXT BOOKS:**

1. Hideharu Amano, "Principles and Structures of FPGAs" Springer Nature Singapore Pte Ltd. 2018
2. S. Brown, R. Francis, J. Rose, Z.Vransic, "Field Programmable Gate array", BSP, 2007.
3. Ronald J . Tocci, Neal S. Widmer, Gregory L. Moss "Digital Systems", 10/e, Pearson academic press 2011.
4. P.K.Chan& S. Mourad, "Digital Design Using Field Programmable Gate Array", PHI, 1994.

**SUGGESTED READING:**

1. P.K. Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Pearson Education 2009.
2. S. Trimberger, Edr., "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.

**26ECE203**

## SILICON PHOTONICS

(Program Elective - I)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITES:** Electromagnetic Theory, Semiconductor Devices, Optical Communication

**COURSE OBJECTIVES:**

**This course aims to:**

1. Understand the fundamentals of silicon photonics including material properties, photonic integrated circuits, and optical wave guiding principles.
2. Analyze and design photonic devices such as passive components (couplers, filters) and active devices (modulators, detectors).
3. Apply silicon photonics in real-world systems like optical communication, sensing and emerging technologies.

**COURSE OUTCOMES:**

**Upon successful completion of the course, the student will be able to:**

1. Understand silicon as a photonic material platform and fundamentals of photonic integrated circuits.
2. Analyze optical wave propagation in dielectric waveguides using electromagnetic principles.
3. Design and evaluate passive silicon photonic components.
4. Analyze and assess active photonic devices.
5. Apply silicon photonics concepts in communication, sensing and emerging systems.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 1 | 1 | 1 |
| **CO2** | 3 | 3 | 2 | 3 | 2 |
| **CO3** | 3 | 3 | 3 | 2 | 3 |
| **CO4** | 3 | 3 | 3 | 3 | 3 |
| **CO5** | 3 | 3 | 3 | 3 | 3 |

**UNIT – I**

**Fundamentals of Silicon Photonics**

This unit covers photonics versus electronics, optical properties of silicon including band structure, refractive index, and transparency window, silicon-on-insulator (SOI) platform, and photonic integrated circuits (PICs).

**UNIT – II**

**Optical Waveguides**

This unit includes Maxwell's equations in waveguides, planar and channel waveguides, single-mode and multimode propagation, effective index method, and loss mechanisms such as absorption and scattering.

**UNIT – III**

**Passive Photonic Devices**

This unit covers coupled mode theory, directional couplers, multimode interference (MMI) devices, Bragg gratings and filters, and power splitters and combiners.

**UNIT – IV**

**Active Photonic Devices and Fabrication**

This unit includes modulators such as electro-optic and thermo-optic types, Mach–Zehnder interferometer (MZI), ring resonators, optical switches and attenuators, and photodetectors, along with CMOS fabrication process overview, lithography and etching, fiber-to-chip coupling including grating couplers and tapers, and packaging and testing.

**UNIT – V**

**Applications and Emerging Trends**

This unit includes optical interconnects, data communication systems, biosensors and lab-on-chip, and quantum photonics and AI hardware.

**TEXT BOOKS:**

1. G. T. Reed and A. P. Knights, *Silicon Photonics: An Introduction*, Wiley
2. L. Vivien and L. Pavesi, *Handbook of Silicon Photonics*, CRC Press
3. J. E. Bowers and C. A. Burrus, *Silicon Photonics*, McGraw Hill

**REFERENCE BOOKS:**

1. B. E. A. Saleh and M. C. Teich, *Fundamentals of Photonics*, Wiley
2. D. K. Mynbaev and L. L. Scheiner, *Fiber-Optic Communications Technology*, Pearson

**26ECE204**

## POWER MANAGEMENT IC DESIGN

(Program Elective - I)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Analog analysis and Digital Design concepts.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Educate about different Power Management circuits for IC.
2. Demonstrate the construction, analysis and design of Linear Regulators
3. Demonstrate the construction, analysis and design of Switching Regulators

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Select and apply appropriate power management circuits for various electronic and VLSI applications.
2. Design and evaluate linear regulators, including LDO architectures.
3. Model and assess the performance of switching regulators under different operating conditions.
4. Examine the stability of switching regulators and design suitable compensation networks to meet performance requirements.
5. Design and integrate key PMIC building blocks such as gate drivers, error amplifiers, ramp generators, and control circuits for efficient power management solutions.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 3 | 3 |
| **CO2** | 3 | 2 | 3 | 3 | 3 |
| **CO3** | 3 | 2 | 3 | 3 | 3 |
| **CO4** | 3 | 2 | 3 | 3 | 3 |
| **CO5** | 3 | 2 | 3 | 3 | 3 |

**UNIT – I**

**Introduction to Power Management:** Application, Need, Discrete vs. Integrated PMIC; DC-DC Converters, Types of DC-DC Converters, Linear versus Switching Regulator, Choosing the Type of Regulator in a Multi-Chip System; Performance Parameters - Efficiency, Accuracy, Line and Load Regulation, Line and Load Transient, PSRR; Remote versus Local Feedback, Point-of-Load Regulator, Kelvin Sensing, Droop Compensation; Current Regulators and their Applications. Sub-1-volt Bandgap Reference.

**UNIT – II**

**Introduction to Linear Regulator**: Applications of Linear Regulator; Parasitic Capacitances in a MOS transistor, Finding the Poles of the Error Amplifier; Stabilising a Linear Regulator - Frequency Compensation Techniques, Dominant Pole Compensation.. Miller Compensation, R.H.P. zero due to Miller Compensation, Reducing the Effect of R.H.P. zero; LDO with NMOS Pass Element; Load Regulation and Output Impedance of LDO; Line Regulation and PSRR of LDO; Sources of Error in a Regulator, Static Offset Correction, Dynamic Offset Cancellation.

Digital LDO, Avoidance of Limit-Cycle Oscillations in a Digital LDO, Hybrid LDO; Short-Circuit Protection and Foldback Current Limit in an LDO.

**UNIT – III**

**Basic Concept of a Switching Regulato**r: Inductor volt-second Balance, Power Stage of a Buck Converter and Calculation of Duty Cycle; Transformer Model of a Buck Converter, Resistive Losses, Efficiency of a Switching Regulator, Efficiency considering only Conduction Losses; Synchronous and Non Synchronous Switching Converters; PWM Control Techniques (Voltage-Mode and Current-Mode Control); Losses in Switching DC-DC Converter- Conduction Loss, Gate-Driver Switching Loss, Segmented Power FETs, Dead-Time Switching Loss, Hard Switching Loss, Magnetic Loss, Relative Significance of Losses as a Function of the Load Current; Inductor Current Ripple and Output Voltage Ripple in a DC-DC Converter, Ripple Voltage versus Duty Cycle, Ripple Voltage versus Input Supply Voltage; Choosing the Inductor and Capacitor of a Buck Converter; Continuous and Discontinuous Conduction Modes - Boundary Condition, Voltage Conversion Ratio in DCM; Classification of Pulse Width Modulators - Trailing, Leading and Dual-Edge PW Modulators; Control Techniques for DC-DC Converters; Voltage Mode Control, Small-Signal Modeling of a DC-DC Converter.

**UNIT – IV**

**Loop Gain and Stability Analysis** using Continuous-Time Model, Compensating a Voltage-Mode-Controlled Buck Converter; Designing Type-I (Integral), Type-II (PI) and Type-III (PID) Compensators; Implementation of Compensators using Op Amp-RC and Gm-C Architectures, Designing Type-III Compensator using Gm-C Architecture, Ramp Generator with Feed-Forward Line Compensation, Loop Gain Compensation via Gm-modulation;

Designing a Buck Converter - Power Loss Budgeting, Sizing of Power FETs, Estimation of Switching Losses and Choice of Switching Frequency, Choosing the External Passive Components (L and C); Capacitor Characteristics, Reducing the Effect of Capacitor ESL.

**UNIT – V**

**Designing the Gate-Drive**r (Gate Buffer and Non-Overlap Clock Generator), Designing the Ramp Generator in a PulseWidth Modulator, Design Considerations of the Error Amplifier; Delays Associated with Pulse-Width Modulators; PFM/PSM for Light Load, Using PSM in CCM to Avoid Duty Cycle Saturation; DCM Operation using an NFET; Designing a Zero-Cross Detector/Comparator.

**TEXT BOOKS:**

1. Abdul Khadeer, “Power Management IC”, NPTEL, Course.
2. Bernhard Wicht., “Design of power management integrated circuits”, Wiley, 2024.

**SUGGESTED READING:**

1. Power Management IC (PMIC) Guide for Automotive, Texas Instruments, 2014.
2. Power Management Techniques for Integrated Circuit Design, Chen, Ke-Horng, Wiley – IEEE, July, 2016

**26ECE205**

## SYSTEM ON CHIP ARCHITECTURE

(Program Elective - II)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE**: Digital Design, Microprocessors and Computer System Architecture

**COURSE OBJECTIVES:**

**This course aims to:**

1. Understand SoC architecture with processor, memory, hardware and software Co-Design.
2. Comprehend the concepts of Processors and memory design.
3. Learn Low Power Design and Verification of SoC

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Understand SoC Fundamentals
2. Analyze Processor Architectures.
3. Analyze Memory Systems for System-on-Chip.
4. Apply Low Power Design Techniques
5. Develop Verification Strategies

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 1 | 2 | 3 | 2 | 1 |
| **CO2** | 2 | 2 | 3 | 2 | 1 |
| **CO3** | 2 | 2 | 3 | 2 | 1 |
| **CO4** | 3 | 2 | 3 | 3 | 1 |
| **CO5** | 3 | 3 | 3 | 3 | 2 |

**UNIT - I**

**Introduction to the Systems Approach**: System Architecture: An Overview, Components of the System: Processors, Memories, and Interconnects, , Hardware-Software Co-Design, Processor Architectures, Memory and Addressing, System-Level Interconnection, SoC Design Flow, EDA Tools for various Phases of SoC Design, SoC Design Challenges.

**UNIT - II**

**Processors:** Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: Minimizing Pipeline Delays, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

**UNIT – III**

**Memory Design: System-on-Chip:** Overview: SOC external memory, Internal Memory, The Size of Memory. Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at Miss Time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual-to-Real Translation, SOC Memory System.

**UNIT - IV**

**Low Power SoC Design:** Low power design fundamentals, Sources of power consumption (dynamic & leakage), Power reduction techniques: Clock gating, Power gating, Dynamic Voltage and Frequency Scaling (DVFS), Adaptive Voltage Scaling (AVS). Multi-VDD and multi-threshold CMOS, Power domains and isolation, Power estimation and verification

**UNIT – V**

**Application Studies:** SOC Design approach, Applications Study: AES algorithms, Image Compression, Video Compression, MP3 Audio Decoding.

**TEXTBOOKS:**

1. Flynn, M.J. and Luk, W., 2011. Computer system design: system-on-chip. John Wiley & Sons.
2. Rochit Rajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000.
3. Rashinkar, P., Paterson, P. and Singh, L., 2002. System-on-a-chip Verification: Methodology and Techniques. Boston, MA: Springer US.

**SUGGESTED READING:**

1. Steve Furber, ARM System on Chip Architecture, 2nd Ed., Addison Wesley Professional, 2000.
2. Jason Andrews, Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology), Newnes, BK and CDROM.
3. Veena S. Chakravarthi, "A practical Approach to VLSI System on Chip (SoC) Design", A comprehensive Guide, Springer.

**26ECE206**

## ADVANCED COMPUTER ARCHITECTURE

(Program Elective - II)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Fundamentals of Computer Architecture.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Understand processor design, instruction formats, and pipelining.
2. Analyze parallel models and performance laws.
3. Apply memory, multiprocessor, and VLSI concepts.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Explain processor design and pipelining.
2. Analyze parallel models and speedup laws.
3. Apply memory hierarchy and cache techniques.
4. Evaluate advanced processor architectures.
5. Design data flow and VLSI systems.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 1 | 2 | 3 | 2 | 1 |
| **CO2** | 2 | 2 | 3 | 2 | 1 |
| **CO3** | 2 | 1 | 3 | 3 | 1 |
| **CO4** | 3 | 2 | 3 | 3 | 2 |
| **CO5** | 3 | 2 | 3 | 3 | 2 |

**UNIT – I**

**Processor Design**: Data Representation, Instruction Formats, Data Path Design: Fixed Point Arithmetic and Floating-Point Arithmetic, CPU Organization, Instruction Pipelining, Super Scalar Techniques, Linear Pipeline Processors, Super Scalar and Super Pipeline Design.

**UNIT – II**

**Parallel Computer Models:** Evolution of Computer architecture, system attributes to performance, Multi processors and multi computers, Multi-vector and SIMD computers, PRAM and VLSI models-Parallelism in Programming, conditions for Parallelism-Program Partitioning and Scheduling-program flow Mechanisms-Speed up performance laws-Amdahl‘s law, Gustafson‘s law-Memory bounded speedup Model.

**UNIT – III**

**Memory Systems and Buses:** Memory hierarchy-cache and shared memory concepts-Cache memory organization-cache addressing models, Aliasing problem in cache, cache memory mapping techniques-Shared memory organization-Interleaved memory organization, Lower order interleaving, Higher order interleaving. Backplane bus systems-Bus addressing, arbitration and transaction.

**UNIT – IV**

**Advanced Processors and Multi-Processor:** Instruction set architectures-CISC and RISC scalar processors-Super scalar processors-VLIW architecture- Multi vector and SIMD computers-Vector processing principles-Cray Y-MP 816 system-Inter processor communication. Multiprocessor system interconnects- Cross bar switch, Multiport Memory-Hot spot problem, Message passing mechanisms-Pipelined Processors-Linear pipeline, on linear pipeline- Instruction pipeline design-Arithmetic pipeline design.

**UNIT – V**

**Data Flow Computers and VLSI Computations:** Data flow computer architectures-Static, Dynamic-VLSI Computing Structures-Systolic array architecture, mapping algorithms into systolic arrays, Reconfigurable processor array-VLSI matrix arithmetic processors-VLSI arithmetic models, partitioned matrix algorithms, matrix arithmetic pipelines.

**TEXT BOOKS:**

1. Carl Hamacher, Vranesic, Zaky, "Computer Organization", 6$^{th}$edition, MGH, 2012
2. William Stallings, "Computer Organization and Architecture designing for Performance", 10$^{th}$edition, PHI, 2016.
3. Kai Hwang, Advanced Computer architecture Parallelism, scalability ,Programmability, Mc Graw Hill, N.Y, 2016
4. Kai Hwang and F.A.Briggs, Computer architecture and parallel processor ' Mc Graw Hill, N.Y, 1999

**SUGGESTED READING:**

1. John L. Hennessy and David A. Patterson, "Computer Architecture", A quantitative Approach, 6$^{th}$ Edition, Elsevier, 2017.
2. Hayes John P, "Computer Architecture and organization" 3$^{rd}$ Edition, MGH, 1998.

**26ECE207**

## HIGH PERFORMANCE COMPUTATION SYSTEMS

(Program Elective - II)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITES:** Programming Fundamentals, Data Structures, Computer Architecture, Operating Systems Basics, Basic knowledge on Linux.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Introduce architecture of modern high performance computing systems.
2. Understand shared and distributed memory parallel programming paradigms.
3. Learn performance optimization techniques.
4. Develop programs using MPI, OpenMP, CUDA and OpenACC.
5. Apply HPC techniques to engineering problems.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Understand HPC architecture and parallel computer organization
2. Apply Python and C for scientific computing
3. Analyze and optimize computational performance
4. Develop MPI, OpenMP, CUDA, OpenACC programs
5. Solve engineering problems using HPC

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 1 | 1 | 3 | 1 |
| **CO2** | 2 | 1 | 1 | 3 | 1 |
| **CO3** | 2 | 1 | 1 | 3 | 1 |
| **CO4** | 2 | 1 | 1 | 3 | 1 |
| **CO5** | 2 | 1 | 1 | 3 | 1 |

**UNIT- I**

**Introduction:** Motivating Parallelism, Scope of Parallel Computing, Parallel Programming Platforms: Implicit Parallelism, Trends in Microprocessor and Architectures, Limitations of Memory, System Performance, Dichotomy of Parallel Computing Platforms.

**UNIT- II**

**HPC Architecture:** CPU architecture, Vectorization, Multicore processors, Memory hierarchy, OS basics, RAM, Interconnect networks, Parallel computer classification, Classes of parallelism, Network topologies, GPUs for HPC.

**UNIT- III**

**Programming Foundations:** Python classes, inheritance, modules, pitfalls, arrays in Python, C arrays 1D and multidimensional, programming practices.

**Optimization & Multithreading:**Python and C/C++ optimization, cache locality, Numba acceleration, scaling, Finite Difference Method, Molecular Dynamics, multiprocessing, multithreading.

**UNIT- IV**

**MPI & GPU Programming:** MPI programming, point-to-point communication, collective operations, CUDA programming, CUDA kernels, matrix multiplication, CuPy, OpenACC directives, Laplace equation solution.

**UNIT-V**

**Applications:** FFT, Spectral methods, profiling, ParaView visualization, Cahn–Hilliard equation, Compressible flow, Ising model, Magnetohydrodynamics, Molecular dynamics, Nonlinear Schrödinger equation, XY model.

**TEXT BOOKS:**

1. Ananth Grama, Anshul Gupta, George Karypis, and Vipin Kumar, **"Introduction to Parallel Computing"**, 2nd edition, Addison-Wesley, 2003, ISBN: 0-201-64865-2
2. Jason Sanders, Edward Kandrot, **"CUDA by Example"**, Addison-Wesley, ISBN-13: 978-0-13-138768-3
3. Michael J. Quinn, **"Parallel Programming in C with MPI and OpenMP"**, McGraw-Hill, 2003, ISBN: 0-07-282256-2

**SUGGESTED READING:**

1. Peter S. Pacheco, **"An Introduction to Parallel Programming"**, Morgan Kaufmann, 2011, ISBN: 978-0-12-374260-5
2. Kai Hwang, "Scalable Parallel Computing", McGraw Hill, 1998, ISBN: 0070317984
3. William Gropp, Ewing Lusk, and Anthony Skjellum, **"Using MPI"**, MIT Press, 1999, ISBN: 0-262-57132-3

**26ECE208**

## SCRIPTING LANGUAGES

(Program Elective -II)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Programming concepts of C, OOPS.

**COURSE OBJECTIVES**:

**This course aims:**

1. To introduce the fundamentals of scripting languages and their role in modern computing.
2. To develop programming proficiency in PERL, Ruby, and TCL for solving real-world problems.
3. To enable students to design web-based and event-driven applications using scripting languages.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Understand and differentiate scripting languages from system programming languages.
2. Apply PERL programming concepts for text processing and automation tasks.
3. Develop advanced PERL applications including web-based and system-level scripts.
4. Design and implement Ruby-based applications, including web services and GUI components.
5. Build TCL / Tk based applications using event-driven programming and GUI toolkits.

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 1 | 2 | 2 | 1 | 1 |
| **CO2** | 1 | 2 | 3 | 1 | 1 |
| **CO3** | 1 | 3 | 3 | 1 | 1 |
| **CO4** | 2 | 3 | 3 | 1 | 2 |
| **CO5** | 2 | 3 | 3 | 2 | 2 |

**UNIT – I**

**Introduction to Scripting Languages & Web Scripting:** Scripts vs Programs, Origin and Evolution of Scripting, Characteristics of Scripting Languages, Uses and Applications of Scripting Languages, Web Scripting Concepts, Overview of Scripting Languages (Perl, Ruby, TCL)

**UNIT – II**

**PERL Programming Fundamentals:** PERL Basics: Names and Values, Variables, Scalar Expressions, Control Structures, Arrays, Lists, Hashes, Strings and Pattern Matching, Regular Expressions, Subroutines.

**UNIT – III**

**Advanced PERL Programming:** Advanced Looping Techniques, File System Handling
pack() and unpack(), eval Function, Data Structures and Modules, Object-Oriented PERL, System Interface, Internet Programming (CGI, Web Applications), Security Issues.

**UNIT – IV**

**Ruby Programming and Applications:** Introduction to Ruby and Rails, Structure and Execution of Ruby Programs, Ruby Gems Package Management, Web Programming in Ruby
CGI Scripts, Cookies Web Servers, SOAP, Web Services, RubyTk Widgets, Events, Canvas, Scrolling.

**UNIT – V**

**TCL and Tk Programming:** TCL Basics: Structure, Syntax, Variables, Control Flow and Data Structures, Input/Output and Procedures, Strings, Patterns, File Handling, Advanced TCL eval, source, exec, uplevel, Namespaces and Error Handling, Event-Driven Programming, Internet-Aware Applications and Security, Tk Toolkit, GUI Concepts, Events and Binding Tk Applications, Perl-Tk Interface.

**TEXT BOOKS:**

1. David Barron – *The World of Scripting Languages*, Wiley,2000
2. David Flanagan & Yukihiro Matsumoto – *The Ruby Programming Language*, O'Reilly Media, Inc, 2008.
3. Randal L. Schwartz, brian d foy, Tom Phoenix. – *Learning Perl, 8th Edition*, O'Reilly Media, Inc. 2025.
4. Brent Welch, Ken Jones, Jeffrey Hobbs – *Practical Programming in Tcl and Tk, Pearson 4th Edition,2003*

**REFERENCE BOOKS**:

1. Larry Wall et al. – *Programming Perl, 4th Edition*, O'Reilly
2. Dave Thomas et al. – *Programming Ruby (Pickaxe Book)*, latest editions (updated for Ruby 3.x trends)
3. E. Quigley – *Perl by Example*, Pearson
4. J. Lee & B. Ware – *Open Source Web Development using LAMP*, Pearson
5. J. P. Flynt – *Perl Power*, Cengage

**26MEM101**

## RESEARCH METHODOLOGY AND IPR

| | |
|---|---|
| Instruction | 2L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 2 |

## COURSE OBJECTIVES:

**This course aims to:**

1. Motivate to choose research as career
2. Formulate the research problem, prepare the research design
3. Identify various sources for literature review and data collection report writing
4. Equip with good methods to analyze the collected data
5. Know about IPR copyrights

## COURSE OUTCOMES:

**Upon completion of this course, students will be able to:**

1. Define research problem, review and asses the quality of literature from various sources
2. Improve the style and format of writing a report for technical paper/ Journal report, understand and develop various research designs.
3. Collect the data by various methods: observation, interview, questionnaires.
4. Analyze problem by statistical techniques: ANOVA, F-test, and Chi-square.
5. Understand apply for patent and copyrights.

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 1 | 2 | 1 |
| **CO2** | 3 | 3 | 3 | 1 | 1 |
| **CO3** | 3 | 2 | 2 | 1 | 1 |
| **CO4** | 3 | 1 | 2 | 2 | 1 |
| **CO5** | 3 | 3 | 3 | 1 | 1 |

### UNIT - I

**Research Methodology:** Research Methodology: Objectives and Motivation of Research, Types of Research, research approaches, Significance of Research, Research Methods verses Methodology, Research Process, Criteria of Good Research, Problems Encountered by Researchers in India, Benefits to the society in general. Defining the Research Problem: Selection of Research Problem, Necessity of Defining the Problem

### UNIT - II

**Literature Survey Report Writing:** Literature Survey: Importance and purpose of Literature Survey, Sources of Information, Assessment of Quality of Journals and Articles, Information through Internet. Report writing: Meaning of interpretation, layout of research report, Types of reports, Mechanics of writing a report. Research Proposal Preparation: Writing a Research Proposal and Research Report, Writing Research Grant Proposal

**UNIT- III**

**Research Design:** Research Design: Meaning of Research Design, Need of Research Design, Feature of a Good Design, Important Concepts Related to Research Design, Different Research Designs, Basic Principles of Experimental Design, Developing a Research Plan, Steps in sample design, types of sample designs.

**UNIT - IV**

**Data Collection and Analysis:** Data Collection: Methods of data collection, importance of Parametric, non parametric test, testing of variance of two normal population, use of Chi-square, ANOVA, Ftest, z-test.

**UNIT - V**

**Patents and Copyright:** Patent: Macro economic impact of the patent system, Patent document, How to protect your inventions. Granting of patent, Rights of a patent, how extensive is patent protection. Copyright: What is copyright. What is covered by copyright? How long does copyright last? Why protect copyright? Related Rights: what are related rights? Enforcement of Intellectual Property Rights: Infringement of intellectual property rights, Case studies of patents and IP Protection.

**TEXT BOOKS:**

1. C.R Kothari, "Research Methodology, Methods & Technique"; New Age International Publishers, 2004
2. R. Ganesan, "Research Methodology for Engineers", MJP Publishers , 2011
3. Y.P. Agarwal, "Statistical Methods: Concepts, Application and Computation", Sterling Publs., Pvt., Ltd., New Delhi, 2004.

**SUGGESTED READING:**

1. Ajit Parulekar and Sarita D' Souza, "Indian Patents Law – Legal & Business Implications"; Macmillan India ltd , 2006
2. B. L.Wadehra; "Law Relating to Patents, Trade Marks, Copyright, Designs & Geographical Indications"; Universal law Publishing Pvt. Ltd., India2000.
3. P. Narayanan; "Law of Copyright and Industrial Designs"; Eastern law House, Delhi 2010.

**26ECC203**

## ANALOG CMOS VLSI DESIGN LAB

| | |
|---|---|
| Instruction | 2P Hours per week |
| Duration of SEE | -- |
| SEE | -- |
| CIE | 50 Marks |
| Credits | 1 |

**COURSE OBJECTIVES:**

**This course aims to:**

1. Skill the students on the Analog IC Design Flow from Design to generation of GDS.
2. Introduce the design procedure of Basic Analog Circuits.
3. Provide hands on use of simulation tools for Analog IC testing

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Characterize a given MOSFET and extract its parameters.
2. Design Basic Analog Circuits using MOSFET.
3. Use Simulation tools to extensively simulate and verify the working of the circuits.
4. Develop quality Layouts for the designed Circuits
5. Communicate his work in the form of a professional report.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 3 | 3 | 3 |
| **CO2** | 2 | 3 | 3 | 2 | 3 |
| **CO3** | 3 | 2 | 3 | 3 | 3 |
| **CO4** | 2 | 2 | 3 | 3 | 3 |
| **CO5** | 3 | 3 | 2 | 2 | 3 |

**List of Experiments:**

1. **Characterisation of MOSFET.**
   - Obtain the output and transfer characteristics of a typical 90 nm NMOS device.
   - Determine the effect of varying (i) Drain voltage, (ii) Gate voltage, (iii) Body bias voltage and (iv) Aspect ratio

2. **Extraction of Various MOSFET parameters.**
   For a given MOSFET and biasing condition, experimentally determine
   - Transconductance
   - threshold voltage
   - Overdrive voltage,
   - Small signal output resistance
   - Intrinsic Gain

3. **NMOS Common Source Amplifier.**
   - Construct a common-source amplifier with resistive load for given specifications. .
   - Perform its dc simulation, ac simulation and transient analysis.
   - Determine the mid-band gain, 3-dB frequency, Gain-bandwidth product, and phase angle from the relevant magnitude and phase plots,
   - Replace the resistive load by appropriate active load and observe changes

4. **Basic CMOS Differential Pair.**
    - Construct an NMOS Input Basic Differential Pair
    - Perform DC, Trans and AC Simulations
    - Calculate Differential and Common Mode Gain, CMRR and ICMR

5. **Single Stage Op-Amp.**
    - Construct an NMOS InputSingle Stage Op-Amp
    - Perform DC, Trans and AC Simulations
    - Calculate Differential and Common Mode Gain, CMRR and Slew Rate

6. **Two Stage Op-Amp.**
    - Construct an NMOS Two Single Stage Op-Amp
    - Perform DC, Trans and AC Simulations
    - Calculate Differential and Common Mode Gain, CMRR and Slew Rate
    - Stability, Gain Margin and Phase-Margin w/o Miller Compensation
    - Stability, Gain Margin and Phase-Margin with FrequencyCompensation

7. **Cascode Op-Amp.**
    - Construct an NMOS Two Single Stage Op-Amp
    - Perform DC, Trans and AC Simulations
    - Calculate Differential and Common Mode Gain, CMRR and Slew Rate
    - Stability, Gain Margin and Phase-Margin w/o Miller Compensation
    - Stability, Gain Margin and Phase-Margin with Frequency Compensation

8. **Construct a Digital to Analog Converter**
    - Perform Trans and AC Simulations
    - Calculate Step Size, VLSB, INL and DNL.
    - Calculate SFDR and ENOB from Simulations

9. **Layout of Static CMOS Inverter**
    - Construct a Basic CMOS Inverter
    - Perform pre-Layout Simulations
    - Development of Layout
    - Perform post-Layout Simulations

10. **Ring Oscillator and Layout**
    - Construct a 3-stage CMOS Ring Oscillator using Inverter designed in Exp-8
    - Perform pre-Layout Simulations
    - Development of Layout
    - Perform post-Layout Simulations

**SUGGESTED READING:**

1. Cadence Design Systems (Ireland) Ltd., “Cadence manual”, 2013.

**26ECC204**

## DIGITAL CMOS VLSI DESIGN LAB

| | |
|---|---|
| Instruction | 2P Hours per week |
| Duration of SEE | -- |
| SEE | -- |
| CIE | 50 Marks |
| Credits | 1 |

**PRE-REQUISITES:** Digital design concepts.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Use MOSFET in the design of Digital Circuits.
2. Learn the fundamental principles of VLSI circuit design in digital domain.
3. Understand the critical design issues of digital logic design.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Understand CMOS Circuit Design
2. Analyze Digital CMOS Circuits
3. Design Sequential Circuits
4. Develop Memory Circuits
5. Implement Physical Layout and Verification

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 1 | 2 | 3 | 2 | 1 |
| **CO2** | 2 | 2 | 3 | 2 | 1 |
| **CO3** | 2 | 2 | 3 | 3 | 1 |
| **CO4** | 2 | 2 | 3 | 3 | 1 |
| **CO5** | 3 | 3 | 3 | 3 | 2 |

**CYCLE I:**

Design the schematic of the given CMOS circuit, perform simulation and analysis of its electrical characteristics, and implement the layout followed by verification using DRC and LVS

1. CMOS Inverter
2. CMOS NAND Gate, NOR Gate
3. 2:1 Multiplexer using Transmission Gate
4. Buffer
5. Dynamic CMOS Logic Gate
6. CMOS SR Latch
7. CMOS D Flip-Flop (Master-Slave)
8. 6T SRAM Cell

**CYCLE II:**

Design the RTL, perform synthesis, Simulation, carry out physical design, and analyze timing, power, and area

1. Half Adder and Full Adder
2. Carry Look-Ahead Adder
3. Comparator
4. Register (Shift Register / Parallel Register)
5. Counter (Up/Down Counter)
6. Finite State Machine (FSM)
7. Arithmetic Logic Unit
8. Multiplier (Array / Booth)

**Note: A minimum of ten experiments should be performed from the list.**

**SUGGESTED READING:**

1. Cadence Design Systems (Ireland) Ltd., "Cadence manual", 2013.

**26ECC205**

## MICROCONTROLLERS AND PROGRAMMABLE DSP LAB

| | |
|---|---|
| Instruction | 2P Hours per week |
| Duration of SEE | -- |
| SEE | -- |
| CIE | 50 Marks |
| Credits | 1 |

**PREREQUISITE:** Programming in C, Basics of Microcontrollers and Digital Signal Processing.

**COURSE OBJECTIVES:**

**This course aims:**

1. To develop embedded C programs for ARM Cortex-M4 based microcontrollers.
2. To interface peripherals and implement serial communication protocols.
3. To implement basic DSP algorithms for real-time signal processing applications.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Install, configure, and utilize development tools for ARM Cortex-M4 based systems.
2. Develop embedded C programs for ARM Cortex-M4 microcontrollers.
3. Interface and control peripherals such as GPIO, ADC, PWM, timers, and interrupts.
4. Implement serial communication protocols such as UART, SPI (SSI), and I2C.
5. Implement DSP algorithms such as convolution, FIR, and IIR filters using C.

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 1 | 3 | 1 | 1 |
| **CO2** | 2 | 1 | 3 | 1 | 1 |
| **CO3** | 2 | 1 | 3 | 2 | 1 |
| **CO4** | 2 | 1 | 3 | 2 | 1 |
| **CO5** | 2 | 1 | 3 | 2 | 3 |

**List of Experiments:**

**PART A**

***Experiments to be carried out on Tiva C Series TM4C123G ARM Cortex-M4 Microcontroller starter kit.***

1. Blink an LED using software delay and using SysTick timer.
2. System clock real-time alteration using the PLL modules.
3. Interface Switch and control an LED using polling method and interrupt method.
4. Control intensity of an LED using PWM implemented in software and hardware.
5. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
6. Temperature indication on an RGB LED.
7. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
8. UART Echo Test.
9. Display sensor data using UART.
10. I2C communication: Interface with a sensor.
11. SPI (SSI) communication: Transmit data to an external device.

**PART B**

***Experiments to be carried out on DSP C6748 evaluation kits and using Code Composer Studio (CCS)***

1. Develop simple assembly and C programs to study the impact of parallel, serial and mixed execution.
2. Implementation of convolution of two sequences.
3. Design and Implementation of FIR filter.
4. Design and Implementation of IIR filter.
5. Basic noise removal application using filtering techniques.

**Note: Any ten experiments should be carried out.**

**TEXT BOOKS:**

1. Yifeng Zhu, "Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C", 4th Edition, 2023.
2. Jonathan W. Valvano, "Embedded Systems: Real-Time Interfacing to ARM Cortex-M Microcontrollers", Latest Edition, 2024.
3. Cem Ünsalan, M. Erkin Yücel, H. Deniz Gürhan, "Digital Signal Processing using ARM Cortex-M Microcontrollers: Theory and Practice", ARM Education (latest resources).

**SUGGESTED READING:**

1. Trevor Martin, "The Insider's Guide to ARM Cortex-M Development", Packt, 2023.
2. ARM Education, "Fundamentals of System-on-Chip Design on ARM Cortex-M Microcontrollers", 2023 Edition.
3. Donald S. Reay, "Digital Signal Processing using ARM Cortex-M4" (practical DSP reference).

**26ECC214**

## AI WORKSHOP FOR ES AND VLSI DESIGN

| | |
|---|---|
| Instruction | 2P Hours per week |
| Duration of SEE | -- |
| SEE | -- |
| CIE | 50 Marks |
| Credits | 1 |

**PREREQUISITE:** None.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Introduce AI tools and machine learning techniques for solving engineering problems, data analysis, and visualization without extensive programming requirements.
2. Provide fundamental knowledge of AI applications in Embedded Systems and VLSI Design, including optimization, prediction, classification, and anomaly detection.
3. Develop the ability to design and implement AI-based solutions for real-world embedded and VLSI engineering applications.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Use AI-assisted tools for data analysis, visualization, and basic engineering applications.
2. Apply machine learning techniques for classification, regression, and anomaly detection in engineering datasets.
3. Develop AI-based solutions for embedded systems, including signal processing and sensor data analysis.
4. Analyze and apply AI techniques to VLSI problems such as power estimation, timing prediction, and design optimization.
5. Design and implement a mini-project integrating AI with Embedded Systems or VLSI Design and present results effectively.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 1 | 1 | 2 | 1 |
| **CO2** | 1 | 1 | 1 | 1 | 1 |
| **CO3** | 1 | 1 | 1 | 2 | 2 |
| **CO4** | 2 | 1 | 1 | 2 | 2 |
| **CO5** | 1 | 1 | 2 | 2 | 2 |

**List of Experiments:**

**1. AI Tool Familiarization & No-Code Setup**

**Tools:** Google Colab, ChatGPT

**Experiment:**

Run a pre-built notebook

Use AI prompts to understand datasets

**Outcome:** Learn AI-assisted workflow

**AI Use:** Generate explanations + summarize outputs

**2.** Data Handling for Embedded Signals
**Tools:** Pandas (via AI-generated code)
**Experiment:**
Load embedded sensor datasets (temperature, humidity, vibration), AI-assisted cleaning & summary
**Outcome:** Data preprocessing basics for Embedded

3. Visualization of Embedded Signals
**Tools:** Matplotlib
**Experiment:**
Plot sensor signals, digital waveforms, and characteristics
Compare embedded system behaviors
**Outcome:** Signal visualization basics

**4.** AI-Based Embedded Classification
**Tools:** Scikit-learn
**Experiment:**
Classify sensor conditions (normal/faulty/noisy)

**Outcome:** ML classification basics for hardware applications

**5. Regression for Sensor Prediction**

**Tools:** Scikit-learn
**Experiment:**

Predict temperature/voltage trends

**Outcome:** Learn prediction models
**AI Use:** Model building + result explanation

**6. AI-Based Fault Detection in Systems**

**Tools:** Scikit-learn
**Experiment:**

Detect anomalies in dataset

**Outcome:** Fault detection basics
**AI Use**: Auto anomaly detection code

**7. Edge AI Simulation**

**Tools:** TensorFlow Lite
**Experiment:**

Convert ML model to lightweight format

**Outcome:** Understand embedded AI deployment
**AI Use:** Model conversion guidance

**8. AI for Image-Based Chip Inspection**

**Tools:** TensorFlow
**Experiment:**

Classify defective vs non-defective chip images

**Outcome:** AI in VLSI manufacturing
**AI Use:** Build CNN with prompts

**9. Power Consumption Prediction (VLSI)**

**Tools:** Pandas
**Experiment:**

Predict power vs frequency/voltage

**Outcome:** AI-driven optimization
**AI Use:** Feature selection + modeling

**10. AI-Assisted Verilog Code Generation**

**Tools:** Icarus Verilog, ChatGPT
**Experiment**:

Generate Verilog (adder, counter)

Simulate outputs

**Outcome:** AI in HDL design
**AI Use:** Code + testbench generation

**11. AI for Timing & Delay Prediction**

**Tools:** Python
**Experiment:**

Model delay vs load/capacitance
**Outcome:** Timing estimation basics
**AI Use:** Regression modelling

**12. TinyML for Embedded Systems**

**Tools:** TensorFlow Lite
**Experiment:**

Simulate microcontroller inference
**Outcome:** AI on constrained devices
**AI Use:** Model compression

**13. AI-Based Design Space Exploration**

**Tools:** Scikit-learn

**Experiment:**

Optimize area, speed, power trade-offs

**Outcome:** VLSI optimization insight
**AI Use:** Parameter tuning

**14. Mini Project (Integrated AI Application)**

**Tools:** All above

**Experiment Options:**

Fault detection system

Signal classifier

Power prediction model

**Outcome:** End-to-end AI application using Jetson Nano

**AI Use:** Full pipeline development + report generation.

**Note: Any ten experiments should be carried out.**

**TEXT BOOKS:**

1. Ian Good fellow, *Deep Learning*, MIT Press, 1st Edition
2. Aurélien Géron, *Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow*, O'Reilly Media, 2nd Edition
3. Simon Monk, *Programming Embedded Systems*, McGraw-Hill, 2nd Edition
4. Neil H. E. Weste, *CMOS VLSI Design: A Circuits and Systems Perspective*, Pearson, 4th Edition

**CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)**

## R26 Curriculum (with effect from AY 2026-27)

**M.E (Embedded Systems & VLSI Design)**

**SEMESTER – II**

| S.no | Course Code | Title of the Course | Scheme of Instruction | | | Scheme of Examination | | | Credits |
|---|---|---|---|---|---|---|---|---|---|
| | | | Hours per week | | | Duration of SEE in Hours | Maximum Marks | | |
| | | | L | T | P/D | | CIE | SEE | |
| **THEORY** | | | | | | | | | |
| 1 | 26ECC206 | IoT and RTOS based Embedded System Design | 3 | -- | -- | 3 | 40 | 60 | 3 |
| 2 | 26ECC207 | VLSI Design Verification and Testing | 3 | -- | -- | 3 | 40 | 60 | 3 |
| 3 | 26ECC215 | AI for Embedded System and VLSI Design | 2 | -- | -- | 3 | 40 | 60 | 2 |
| 4 | | Program Elective-III | 3 | -- | -- | 3 | 40 | 60 | 3 |
| 5 | | Program Elective-IV | 3 | -- | -- | 3 | 40 | 60 | 3 |
| 6 | | Audit Course-II | 2 | -- | -- | 2 | -- | 50 | Non-Credit |
| **PRACTICALS** | | | | | | | | | |
| 7 | 26ECC208 | IoT and RTOS Lab | -- | -- | 2 | -- | 50 | -- | 1 |
| 8 | 26ECC209 | RTL Synthesis, Simulation and verification Lab | -- | -- | 2 | -- | 50 | -- | 1 |
| 9 | 26ECC210 | Mini Project | -- | -- | 2 | -- | 50 | -- | 1 |
| 10 | 26ECC211 | Industrial Internship / Training | 90 Hours | | | -- | 50 | -- | 1 |
| **Total** | | | **16** | **--** | **6** | **17** | **400** | **350** | **18** |
| **Clock Hours Per Week: 22** | | | | | | | | | |

**L: Lecture** **D: Drawing** **CIE: Continuous Internal Evaluation**

**T: Tutorial** **P: Practical/Mini Project / Dissertation** **SEE: Semester End Examination**

**26ECC206**

## IoT AND RTOS BASED EMBEDDED SYSTEM DESIGN

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Basic knowledge of electronics, microcontrollers, C programming, communication protocols, networking, and operating system fundamentals.

## COURSE OBJECTIVES:

**This course aims:**

1. To understand the fundamentals, architecture, and communication models of Internet of Things (IoT) systems.
2. To develop skills in designing IoT-based embedded systems using sensors, devices, and data analytics tools.
3. To gain knowledge of Real-Time Operating Systems (RTOS) concepts and their application in embedded system design.

## COURSE OUTCOMES:

**Upon completion of this course, students will be able to:**

1. Understand the concepts, architecture, and communication mechanisms of IoT systems.
2. Apply IoT design methodology to develop real-world applications and case studies.
3. Analyze IoT devices, platforms, and data analytics tools for efficient system implementation.
4. Evaluate scheduling algorithms and real-time constraints in RTOS-based systems.
5. Design and implement RTOS-based embedded applications using multitasking and synchronization techniques.

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 1 | 2 | 2 | 1 |
| **CO2** | 2 | 2 | 2 | 2 | 1 |
| **CO3** | 3 | 2 | 3 | 2 | 2 |
| **CO4** | 3 | 2 | 3 | 3 | 2 |
| **CO5** | 3 | 3 | 3 | 3 | 2 |

## UNIT-I

**Introduction to Internet of Things:** Overview, definitions, and characteristics of IoT; physical and logical design aspects of IoT; functional blocks of IoT; communication models and APIs; IoT levels and deployment templates.

**Tools for IoT:** Introduction to tools such as Chef and Puppet, along with their respective case studies; NETCONF-YANG and related case studies.

## UNIT-II

**IoT Physical Devices and End Points:** Fundamental building blocks of IoT devices; overview of the Raspberry Pi board and its interfaces (Serial, SPI, I2C); introduction to the BeagleBone Black board and its internal architecture.

**Data Analytics for IoT:** Concepts of Apache Hadoop; use of MapReduce for batch data processing; Apache Oozie; Apache Spark; Apache Storm; real-time data analytics using Apache Storm.

**UNIT-III**

**IoT Platform Design Methodology:** Design methodology for IoT systems; case study on IoT-based weather monitoring systems.

**Case Studies on IoT Design:** Applications including home automation, smart parking, weather monitoring systems, weather reporting Bots, Air pollution monitoring, Forest fire detection, smart irrigation, and IoT-based printers.

**UNIT-IV**

**RTOS Concepts:** Comparison between traditional operating systems and real-time operating systems; real-time system concepts; classification of hard and soft real-time systems with examples; jobs and processors; timing constraints (hard and soft); classical uniprocessor scheduling algorithms such as RMS and preemptive EDF; considerations for preemption and exclusion conditions.

**UNIT-V**

**Introduction to VxWorks:** RTOS kernel concepts and multitasking issues; task assignment and task switching; foreground interrupt service routines (ISRs) and background tasks; critical sections; POSIX real-time extensions in VxWorks; timeout features; task creation; synchronization mechanisms including semaphores (binary and counting), mutex, mailbox, and message queues.

**Case Study:** Automatic vending machine for embedded system design

**TEXT BOOKS:**

1. Arshdeep Bahga and Vijay Madisetti, “Internet of Things - A Hands-on Approach, Universities Press", 2015.
2. Jane W.S.Liu, “Real Time Systems”, Pearson Education, Asia, 2018.
3. Wind River Systems Inc., “VxWorks Programmers Guide”, 2019.

**SUGGESTED READING:**

1. C. M. Krishna and Kang G. Shin, *Real-Time Systems*, McGraw-Hill, 1st Edition (Reprint 2017).

**26ECC207**

## VLSI DESIGN, VERIFICATION AND TESTING

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Knowledge of Analog and Digital CMOS VLSI Design, C and C++ Language concepts.

**COURSE OBJECTIVES:**

**This course aims:**

1. To understand SystemVerilog concepts and verification methodologies for digital systems.
2. To develop verification environments using OOP, interfaces, assertions, and randomization techniques.
3. To apply testing and design-for-testability techniques for VLSI circuits.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Use SystemVerilog data types, arrays, tasks, and functions to develop verification programs.
2. Apply object-oriented programming concepts to create reusable verification components.
3. Develop testbenches using interfaces, assertions, and simulation-based verification techniques.
4. Implement constrained randomization and functional coverage for effective verification.
5. Analyze fault models and apply ATPG and DFT techniques for testing digital circuits.

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 2 | 2 | 1 |
| **CO2** | 3 | 1 | 2 | 3 | 1 |
| **CO3** | 3 | 1 | 2 | 3 | 1 |
| **CO4** | 3 | 1 | 2 | 2 | 1 |
| **CO5** | 3 | 1 | 2 | 3 | 1 |

**UNIT – I**

**Verification Guidelines:** Verification Process, Basic Test Bench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Test Bench Components, Layered Test Bench, Building Layered Test Bench, Simulation Environment Phases, Test Bench Performance.

**Data Types:** Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Creating New Types With Typedef, Creating User-Defined Structures, Type Conversion, Enumerated Types, Constants Strings. Procedural Statements and Routines: Procedural Statements, Tasks, Functions and Void Functions. Write programs on above with examples.

**UNIT – II**

**Basic OOPS:** Introduction, First Class, Define a Class, OOP Terminology, Creating New Objects, Object De- Allocation, Using Objects, Static Variables Vs. Global Variables, Class Methods, Defining Methods Outside of the Class, Scoping Rules, Using One Class Inside Another. Write programs on above with examples

**UNIT – III**

**Connecting the Test Bench and Design:** Separating the Test Bench and Design, Interface Constructs, Stimulus Timing, Interface Driving and Sampling, Connecting it all Together, Top-Level Scope Program Module Interactions. System Verilog Assertions, Understanding Dynamic Objects, Copying Objects.

**UNIT – IV**

**Randomization:** Introduction, What to Randomize, Randomization in System Verilog, Constraint Details Solution Probabilities, Controlling Multiple Constraint Blocks, Valid Constraints, In-Line Constraints, The Pre Randomize and Post Randomize Functions, Random Number Functions, Constraints Tips and Techniques, Common Randomization Problems, Iterative and Array Constraints.

**UNIT – V**

**Simulation Based Verification and Testing:** Fault Simulation: Parallel, Deductive, Concurrent, Functional Testing Methodologies: Exhaustive Testing, Pseudo-Exhaustive Testing,

**Structure based Testing:** Fault Model based Testing, Stuck-at Faults, Bridging Faults, Stuck-Open Faults, Delay Faults Fault Grading, Automatic Test Pattern Generation Algorithms: D-Algorithms, PODEM, FAN, etc Design for Testability Methods: Testable Combinational / Sequential Circuits, Scan Path Design, Partial Scan, Built-In Self-Test (BIST), Data Compaction Techniques**.**

**TEXT BOOKS:**

1. Chris Spears, “System Verilog for Verification”, Springer, 2nd Edition 2006.
2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers 2002.
3. Bergeron, Janick. Writing test benches using System Verilog, 1st Edition, Springer Science & Business Media, 2007.

**SUGGESTED READING:**

1. Writing test benches using System Verilog by Janick Bergeron Edition: illustrated Published by Birkhäuser, 2006, ISBN 0387292217, 9780387292212.
2. System Verilog for Verification: A Guide to Learning the Test bench Language Features by Chris Spear Edition: 2, Published by Springer, 2008 ISBN 0387765298, 9780387765297.
3. Vijayaraghavan, Srikanth, and Meyyappan Ramanathan. A practical guide for System Verilog assertions, Springer Science & Business Media, 2006.

**26ECC215**

## AI FOR EMBEDDED SYSTEM AND VLSI DESIGN

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITES:** Embedded Systems Design, Digital VLSI Design , Programming (Python/C), Basics of Machine Learning

**COURSE OBJECTIVES:**

**This course aims:**

1. Understand AI techniques and their applications in Embedded Systems and VLSI Design.
2. Explore optimization and deployment of AI models on resource-constrained embedded and hardware platforms.
3. Design AI-enabled solutions for VLSI automation, hardware acceleration, and real-world embedded applications.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Analyze AI models for embedded constraints.
2. Implement optimized AI algorithms on embedded platforms.
3. Apply AI techniques in VLSI design and verification.
4. Design hardware accelerators for AI workloads.
5. Develop real-time AI-based embedded applications.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 2 | 2 | 1 |
| **CO2** | 2 | 3 | 3 | 3 | 3 |
| **CO3** | 3 | 2 | 3 | 3 | 2 |
| **CO4** | 3 | 2 | 3 | 3 | 2 |
| **CO5** | 2 | 2 | 3 | 3 | 3 |

**UNIT - I**

**Fundamentals of AI for Embedded Systems:** Overview of Artificial Intelligence, Machine Learning, Deep Learning -Embedded Systems vs Intelligent Embedded Systems - Edge AI vs Cloud AI- Constraints: Power, Memory, Latency, Throughput - Introduction to TinyML and edge inference - AI hardware overview (CPU, GPU, TPU, NPU basics)

**UNIT - II**

**Machine Learning Techniques for Embedded Systems:**Supervised and Unsupervised Learning - Feature extraction and selection methods - Lightweight ML algorithms (KNN, Decision Trees, SVM) - Model optimization techniques: Quantization -Pruning -Knowledge Distillation -Deployment pipelines for embedded AI

**UNIT –III**

**Deep Learning Deployment on Embedded Platforms:** CNN and RNN fundamentals for embedded applications-Frameworks: TensorFlow Lite, PyTorch Mobile, ONNX -Embedded platforms: ARM Cortex, RISC-V, FPGA-based systems -Real-time inference and latency optimization -Case studies: Image classification, speech recognition.

**UNIT- IV**

**AI in VLSI Design and Hardware Acceleration:** AI in Electronic Design Automation (EDA) -Placement, routing, and floor planning using ML -Timing and power prediction using AI -Hardware accelerators: GPU, FPGA, ASIC for AI -Introduction to systolic arrays and AI chips -Energy-efficient AI hardware design

**UNIT - V**

**Hardware-Software Co-Design and Applications:** Hardware-software co-design principles-AI workload partitioning -Embedded AI system architecture design- Security and reliability in AI hardware -Applications: Smart IoT systems- Autonomous systems- Healthcare and industrial AI -Emerging trends: Neuromorphic computing, Edge intelligence

**TEXT BOOKS:**

1. Ian Goodfellow, Yoshua Bengio, Aaron Courville, "Deep Learning", MIT Press, 1st Edition, 2016.
2. Pete Warden, Daniel Situnayake, "TinyML: Machine Learning with TensorFlow Lite on Arduino and Ultra-Low-Power Microcontrollers", O'Reilly Media, 1st Edition, 2019.
3. Steve Furber, "ARM System-on-Chip Architecture", Addison-Wesley, 2nd Edition, 2000.

**SUGGESTED BOOKS:**

1. Vivienne Sze, Yu-Hsin Chen, Tien-Ju Yang, Joel Emer, "Efficient Processing of Deep Neural Networks", Morgan & Claypool, 1st Edition, 2020
2. Neil H. E. Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", Pearson, 4th Edition, 2010

**26ECE209**

## DESIGN FOR TESTABILITY

(Program Elective – III)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PRE-REQUISITES:** Analog and Digital design concepts.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Understand the fundamentals of digital circuit modeling, logic simulation, and fault modeling techniques for effective testing.
2. Learn Automated Test Pattern Generation (ATPG), fault simulation methods, and Design for Testability (DFT) techniques including scan architectures and boundary scan standards.
3. Explore Built-In Self-Test (BIST) architectures and advanced self-test strategies for reliable board-level and system-level digital system design.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Understand the concepts of modelling and testing of digital circuits.
2. Modelling of various logic level faults.
3. Learn various testing methods of digital circuits.
4. Explore need for Design for Testability
5. Learn various self-testing architectures and design.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 2 | 3 | 2 |
| **CO2** | 2 | 3 | 3 | 1 | 3 |
| **CO3** | 3 | 3 | 2 | 2 | 3 |
| **CO4** | 2 | 3 | 3 | 3 | 2 |
| **CO5** | 3 | 3 | 2 | 2 | 2 |

**UNIT I**

**Introduction to Test and Design for Testability (DFT) Fundamentals. Modeling**: Modeling digital circuits at logic level, register level and structural models. Levels of modeling. Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

**UNIT II**

**Fault Modeling** – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits

**UNIT III**

**Testing for single stuck faults (SSF)** – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models.

**Vector simulation** – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

**UNIT IV**

**Design for testability** – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

**UNIT V**

**Built-in self-test (BIST)** – BIST Concepts and test pattern generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level.

Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, Embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.

**TEXTBOOKS:**

1. Parag K. Lala, ***An Introduction to Logic Circuit Testing***, Morgan & Claypool Publishers, 2009.
2. Michael L. Bushnell and Vishwani D. Agrawal, ***Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits***, Springer India, 2005.
3. Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, ***VLSI Test Principles and Architectures: Design for Testability***, Morgan Kaufmann Publishers (Elsevier), 2006.

**SUGGESTING READINGS:**

1. Parag K Lal, "Fault Tolerant and Fault Testable Hardware Design" , BS Publications, 2020.
2. Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001
3. Alfred Crouch., Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall. 1999.
4. Robert J. Feugate, Jr., Steven M. Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.

**26ECE210**

# VLSI SIGNAL PROCESSING

(Program Elective-III)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** VLSI Design, Signals and Systems and DSP concepts.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Understand fundamentals of DSP systems. Impart the knowledge of Pipelined and parallel recursive and adaptive filters.
2. Gain knowledge of folding and unfolding transformations for efficient hardware implementation.
3. Study and analyze Systolic architecture design concepts, fast convolution algorithms for efficient signal processing applications.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Understand the concepts of various DSP algorithms, its DFG representation, pipelining and parallel processing approaches.
2. Analyze and implement folding transformations and register minimization techniques in DSP systems.
3. Design and evaluate unfolding transformations and understand their impact on system throughput and critical path.
4. Develop and analyze systolic array architectures for applications like FIR filtering and matrix multiplication.
5. Implement and compare fast convolution algorithms such as Cook-Toom and Winograd for efficient computation.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 1 | 3 | 2 | 1 |
| **CO2** | 3 | 1 | 3 | 2 | 1 |
| **CO3** | 3 | 1 | 3 | 1 | 1 |
| **CO4** | 3 | 1 | 2 | 2 | 1 |
| **CO5** | 3 | 2 | 3 | 1 | 1 |

**UNIT – I**

**Pipelining and Parallel Processing:** Introduction, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for Low Power, Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.

**UNIT – II**

**Folding:** Introduction, Folding, Transform, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.

**UNIT – III**

**Unfolding**: Introduction, an Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming, Applications of Unfolding.

**UNIT – IV**

**Systolic Architecture Design:** Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

**UNIT – V**

**Fast Convolution:** Introduction, Cook, TOOM Algorithm, Winogard Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

**TEXT BOOKS:**

1. Keshab K. Parthi, "VLSI Digital signal processing systems, design and implementation", New Delhi Wiley, Inter Science, 1st edition, 2015.
2. Mohammad Isamail and Terri Fiez, "Analog VLSI signal and information processing", McGraw Hill, 2021.
3. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice, Hall, 1985.

**SUGGESTED READING:**

1. U. Meyer -Baese, Digital Signal Processing with FPGAs, Springer, 2004.
2. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing, Jose E. France, Yannis Tsividis, Prentice Hall, 1994.
3. VLSI Digital Signal Processing, Medisetti V. K., IEEE Press (NY), USA, 1995

**26ECE211**

# ALGORITHMS for VLSI

(Program Elective-III)

| | |
|---|---|
| Instruction | 3L Hours per Week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE**: Basics of VLSI.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Understand the concepts of Physical Design Process such as partitioning, Floor planning Placement and Routing.
2. Discuss the concepts of design optimization algorithms and their application to physical design automation.
3. Understand the concepts of simulation and synthesis in VLSI Design.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Describe and explain the VLSI design flow including logic synthesis and verification stages.
2. Analyze and apply algorithms for partitioning, floor planning, placement, and routing in VLSI physical design.
3. Compare and evaluate various global routing algorithms including maze routing, Steiner tree, and ILP-based approaches.
4. Analyze single-layer, two-layer, and multi-layer detailed routing algorithms.
5. Apply and optimize over-the-cell routing, via minimization, and layout compaction techniques (1D and 2D).

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 1 | 1 | 1 | 1 |
| **CO2** | 1 | 3 | 3 | 2 | 3 |
| **CO3** | 1 | 2 | 2 | 2 | 2 |
| **CO4** | 2 | 2 | 1 | 3 | 2 |
| **CO5** | 1 | 3 | 3 | 2 | 2 |

**UNIT– I**

**Logic Synthesis & Verification:** Introduction to Combinational Logic Synthesis, Binary Decision Diagram, Hardware Models for Gigh-level Synthesis.

**Partitioning:** Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing & Evolution, Other Partitioning Algorithms.

**UNIT– II**

**Placement, Floor Planning & Pin Assignment**: Problem formulation, Simulation base placement algorithms, Other Placement Algorithms, Constraint-Based Floor Planning, Floor Planning Algorithms for Mixed Block & Cell Design. General & Channel Pin Assignment.

**UNIT – III**

**Global Routing**: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithm, Line Probe Algorithm, Steiner Tree Based Algorithms, ILP Based Approaches.

**UNIT– IV**

**Detailed Routing**: Problem Formulation, Classification of Routing Algorithms, Single Layer Routing Algorithms, Two Layer Channel Routing Algorithms, Three Layer Channel Routing Algorithms, and Switchbox Routing Algorithms.

**UNIT– V**

**Over the Cell Routing & Via Minimization**: Two Layers Over the Cell Routers, Constrained & Unconstrained Via Minimization.

**Compaction:** Problem Formulation, One-Dimensional Compaction, Two Dimension-Based Compaction, Hierarchical Compaction.

**TEXT BOOKS:**


1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.
2. Sabih H. Gerez, "Algorithms for VLSI Design Automation", Wiley, 2008.
3. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002.


**SUGGESTED READING:**


1. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
2. Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition.

**26ECE212**

## MIXED SIGNAL AND RF IC DESIGN

(Program Elective-III)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Network Theory, Analog CMOS VLSI Design, Communication Systems.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Understand the principles and operation of mixed-signal circuits, switched-capacitor circuits, and data converters.
2. Analyze the effects of nonlinearity, noise, impedance matching, and high-frequency circuit behavior.
3. Design and evaluate high-frequency amplifiers and low-noise amplifiers for communication and VLSI applications.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Understand the design Comparator, switched capacitor, filters metric of a given RF system.
2. Design and Analyze Nyquist Data converter.
3. Design and Analyze of over-sample Data converter
4. Understand the design of High bandwidth and LNA circuits.
5. Apply techniques for designing amplifiers for high frequencies.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 3 | 2 | 3 | 3 |
| **CO2** | 3 | 2 | 3 | 3 | 3 |
| **CO3** | 3 | 2 | 3 | 3 | 3 |
| **CO4** | 3 | 2 | 3 | 3 | 3 |
| **CO5** | 3 | 2 | 3 | 3 | 3 |

**UNIT – I**

**OP-Amp:**As a Comparator, Charge Injection Error, Switched Capacitor Basic Operation and analysis, First Order Filter, Switched Capacitor Gain Circuits, Sample and Hold Circuit-its Performance.

**UNIT – II**

**Digital to Analog Converter:** Nyquist Rated DAC, Decoder Based Converter, Binary Scaled Converter, Thermometer Coded Converter, Hybrid Converter, Successive Approximation Converter. Analog To Digital Converter: Algorithmic ADC, Flash Converter, Two-Step ADC, Interpolation ADC, Folding, ADC, Piplied ADC, Time Interleaved ADC.

**UNIT – III**

**Oversampled Converter:** Oversampling with and without Noise Shaping, System Architecture, Digital Decimation Filter, High Order Modulation, Band Pass Over Sampling Converter, Multi-Bit Oversampling Converter, Third Order ADC.

**UNIT – IV**

**Nonlinearity and Reflection Coefficient:** Nonlinearity and Time Variance of System, Effects of Non-**Linearity:** Harmonic Distortion, Gain Compression, Cross Modulation, Inter-Modulation, Cascaded Non-Linear Stages,

**Device Noise:** Thermal Noise, Flicker Noise Review, Representation of Noise in Circuits

**Noise:** Noise as a Random Process, Noise Spectrum, Effect of Transfer Function on the Noise, Sensitivity and Dynamic Range, Passive Impedance Transformation: Q, Series to Parallel Conversion, Scattering Parameters,

**UNIT – V**

**High Frequency Amplifier Design:** Bandwidth Estimation using Open-Circuit Time Constants, Bandwidth Estimation using Short-Circuit Time Constants, Rise-Time, Delay and Bandwidth, Zeros to Enhance Bandwidth, Shunt-Series Amplifiers, Tuned Amplifiers, Cascaded Amplifiers, Noise Figure, Intrinsic MOS Noise Parameters.

**Low Noise Amplifiers:** General Considerations, Problem of Input Matching, LNA-Topologies – CS-Stage with Inductive Load, CS-Stage with Resistive Feedback, Common Gate Stage, Cascode CS Stage with Inductive De-Generation.

**TEXT BOOKS:**


1. Behzad Razavi, "RF Microelectronics", Prentice Hall, 1997.
2. Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2004.
3. Analog Integrated Circuit Design, Tony Chan Carusone, David Jhons, Ken Martin, 2nd Edition, Wiley, 2013.


**SUGGESTED READING:**


1. Abidi, P.R. Gray, and R.G. Meyer, eds., "Integrated Circuits for Wireless Communications", New York: IEEE Press, 1999.
2. R. Ludwig and P. Bretchko, "RF Circuit Design, Theory and Applications", Pearson, 2000.

**26ECE213**

## ADVANCED SENSORS AND ACTUATORS FOR EMBEDDED SYSTEMS

(Program Elective-IV)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Basic Electronics, Microcontrollers, Embedded Systems.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Understand principles and classification of advanced sensors and actuators.
2. Explore sensor interfacing techniques with embedded systems.
3. Study smart sensors, MEMS, and IoT-enabled sensing systems.
4. Analyze actuator technologies and control mechanisms.
5. Develop applications integrating sensors and actuators in real-time embedded systems.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Classify and analyze different types of sensors and their characteristics.
2. Design sensor interfacing circuits for embedded applications.
3. Evaluate MEMS and smart sensor technologies.
4. Analyze actuator systems and control strategies.
5. Develop embedded solutions using sensors and actuators.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 1 | 1 | 1 |
| **CO2** | 3 | 2 | 2 | 3 | 2 |
| **CO3** | 2 | 2 | 3 | 3 | 1 |
| **CO4** | 3 | 2 | 2 | 3 | 2 |
| **CO5** | 2 | 2 | 3 | 3 | 3 |

**UNIT – I**

**Introduction to Sensors:** Sensor fundamentals, classification, static and dynamic characteristics, error analysis, calibration techniques, signal conditioning, analog and digital sensors, noise and filtering.

**UNIT – II**

**Advanced Sensors:** Optical sensors, ultrasonic sensors, biosensors, chemical sensors, magnetic sensors, temperature and pressure sensors, smart sensors and sensor fusion techniques.

**UNIT – III**

**MEMS and Smart Sensor Systems:** Introduction to MEMS, fabrication techniques, MEMS sensors (accelerometers, gyroscopes), smart sensor architecture, wireless sensor networks, IoT-based sensing.

**UNIT – IV**

**Actuators and Control:** Classification of actuators, electrical, hydraulic and pneumatic actuators, DC/AC motors, stepper and servo motors, piezoelectric actuators, actuator interfacing and control techniques.

**UNIT – V**

**Embedded Applications:** Sensor-actuator integration, real-time data acquisition, embedded system design for automation, robotics, healthcare and industrial applications, case studies using Arduino/ARM platforms in Automotives Domain and Healthcare systems.

**TEXT BOOKS:**


1. Ramon Pallas-Areny, "Sensors and Signal Conditioning", Wiley, 2000.
2. Jacob Fraden, "Handbook of Modern Sensors", Springer, 2010.
3. H. Baltes et al., "CMOS MEMS: Advanced Microsystems", Wiley, 2005.


**SUGGESTED READING:**


1. John Turner, "Sensor Technology Handbook", Elsevier, 2009.
2. S. E. Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures", CRC Press, 2002.
3. Datasheets and application notes of modern sensors and actuators, latest edition.

**26ECE214**

# INTRODUCTION TO QUANTUM COMPUTING

(Program Elective –IV)

| | |
|---|---|
| Instruction | 3L Hours per Week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

## COURSE OBJECTIVES:

**This course aims to:**

1. Understand the fundamentals, notations, and building blocks of quantum computing along with key quantum algorithms.
2. Gain knowledge of quantum machine learning and quantum deep learning techniques.
3. Apply quantum computing concepts and algorithms to solve computational problems.

## COURSE OUTCOMES:

**After completion of this course, students will be able to:**

1. Understand basic quantum computing concepts, qubits, gates, and quantum operations.
2. Implement fundamental quantum algorithms such as Deutsch-Jozsa, Grover's, and Shor's algorithm using Qiskit.
3. Apply quantum machine learning techniques including regression, clustering, and classification.
4. Develop basic quantum deep learning models using hybrid quantum-classical neural networks.
5. Apply quantum variational and optimization algorithms for real-world problems.

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 3 | 2 | 3 | 3 |
| **CO2** | 3 | 2 | 3 | 3 | 3 |
| **CO3** | 3 | 2 | 3 | 3 | 3 |
| **CO4** | 3 | 2 | 3 | 3 | 3 |
| **CO5** | 3 | 2 | 3 | 3 | 3 |

## UNIT - I

**Introduction to Quantum Computing:**

Quantum Bits, Dirac Notation, Single and Multiple Qubit Gates, No Cloning Theorem, Quantum Interference, Postulates of Quantum Computing - Quantum State, Quantum Evolution, Quantum Measurement, Bell's Inequality Test, Density Coding, Quantum Teleportation, BB84 Protocol, Quantum error correction.

## UNIT - II

**Introduction to Quantum Algorithms:**

Qiskit, Deutsch-Jozsa Algorithm Implementation, Bernstein-Vajirani Algorithm, Simon's Algorithm, Quantum Fourier Transform - QFT implementation in Qiskit, Quantum Phase Implementation, Quantum Phase Estimation in Qiskit, Shor's Period Finding Algorithm, Grover's Search Algorithm.

**UNIT - III**

**Quantum Machine Learning:**

Data Encoding, HHL Algorithm, HHL Algorithm Implementation, Quantum Linear Regression, Quantum Swap Test Subroutine, Swap Test Implementation, Quantum Euclidean Distance Calculation, Quantum K-Means Clustering, Quantum Principal Component Analysis, Quantum Support Vector Machines, SVM Implementation using Qiskit.

**UNIT - IV**

**Quantum Deep Learning:**

Hybrid Quantum-Classical Neural Networks, Classification using Hybrid Quantum-Classification Neural Network, Quantum Neural Network for Classification on Near-Term Processors.

**UNIT - V**

**Quantum Variational Optimization and Adiabatic Methods:**

Variational Quantum Eigen solver, Expectation Computation, Implementation of the VQE Algorithm, Quantum Max-Cut Graph Clustering, Quantum Adiabatic Theorem, Quantum Approximate Optimization Algorithm, Quantum Algorithm for Finance.

**TEXT BOOKS:**


1. Michael A. Nielsen, "Quantum Computation and Quantum Information", Cambridge University Press, 2010.
2. David McMahon, "Quantum Computing Explained", Wiley, 2008.
3. **Chris Bernhardt**, *Quantum Computing for Everyone*, MIT Press, **2019**.


**SUGGESTED READING:**


1. **Michael A. Nielsen, Isaac L. Chuang**, *Quantum Computation and Quantum Information*, Cambridge University Press, **2010 (10th Anniversary Edition)**.
2. **Jack D. Hidary**, *Quantum Computing: An Applied Approach*, Springer, **2021**.
3. **Robert S. Sutor**, *Dancing with Qubits: How quantum computing works and how it can change the world*, Packt Publishing, **2019**.


**E-RESOURCES:**

**Tools:** Qiskit-based programming, https://www.ibm.com/quantum/qiskit

**26ECE215**

## ADVANCED IMAGE AND VIDEO PROCESSING

(Program Elective – IV)

| | |
|---|---|
| Instruction | 3L Hours per Week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Digital Image Processing.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Understand fundamental principles of image and video formation and representation.
2. Apply mathematical and computational techniques for image processing and analysis.
3. Develop knowledge of advanced video processing and coding methods.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Understand the concept of image formation and representation.
2. Know the need of transformation and convolution.
3. Understand the necessity and importance of feature detection and geometric mapping.
4. Know how to do motion estimation in video.
5. Understand the basic ideas of video coding.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 1 | 1 | 2 | 1 |
| **CO2** | 1 | 1 | 1 | 1 | 1 |
| **CO3** | 1 | 1 | 1 | 2 | 2 |
| **CO4** | 2 | 1 | 2 | 2 | 2 |
| **CO5** | 1 | 1 | 2 | 2 | 2 |

**UNIT-I**

**Image Formation and Representation**: 3D to 2D projection, photometric image formation, trichromatic colour representation, video format (SD, HD, UHD, HDR), contrast enhancement (concept of histogram, nonlinear mapping, histogram equalization).

**UNIT-II**

**Review of 1D Fourier Transform and Convolution**: Concept of spatial frequency. Continuous and Discrete Space 2D Fourier transform. 2D convolution and its interpretation in frequency domain. Implementation of 2D convolution. Separable filters. Frequency response. Linear filtering (2D convolution) for noise removal, image sharpening, and edge detection. Gaussian filters, DOG and LOG filters as image.

**UNIT-III**

**Geometric Mapping and Feature Detection**: Geometric mapping (affine, homography), Feature based camera motion estimation (RANSAC). Image warping. Image registration. Panoramic view stitching, Feature detection (Harris corner, scale space, SIFT), feature descriptors (SIFT). Bag of Visual Word representation for image classification.

**UNIT-IV**

**Motion Estimation**: optical flow equation, optical flow estimation (Lucas-Kanade method, KLT tracker); block matching, multi-resolution estimation. Deformable registration (medical applications), Moving object detection (background/foreground separation): Robust PCA (low rank + sparse decomposition). Global camera motion estimation from optical flows. Video stabilization. Video scene change detection.

**UNIT-V**

**Video Coding**: block-based motion compensated prediction and interpolation, adaptive spatial prediction, block-based hybrid video coding, rate-distortion optimized mode selection, rate control, Group of pictures (GoP) structure, trade-off between coding efficiency, delay, and complexity, depth from disparity, disparity estimation, view synthesis. Multiview video compression. Depth camera (Kinect). 360 video camera and view stitching.

**TEXT BOOKS:**


1. R. Szeliski, Computer Vision: Algorithms and Applications, Springer, London, UK, 2nd Edition, 2022, ISBN: 978-3030343712.
2. Y. Wang, J. Ostermann, and Y. Q. Zhang, Video Processing and Communications, Prentice Hall, Upper Saddle River, NJ, USA, 1st Edition, 2002, ISBN: 978-0130175472.
3. R. C. Gonzalez and R. E. Woods, Digital Image Processing, Prentice Hall, (3rd Edition) 2008. ISBN number 9780131687288.


**SUGGESTED READING:**


1. J. C. Russ, The Image Processing Handbook, CRC Press, Boca Raton, FL, USA, 7th Edition, 2016, ISBN: 978-1498740289.
2. R. C. Gonzalez, R. E. Woods, and S. L. Eddins, Digital Image Processing Using MATLAB, Pearson Education, Upper Saddle River, NJ, USA, 2nd Edition, 2009, ISBN: 978-0130085191.

**26ECE216**

## INDUSTRIAL IoT: ARCHITECTURE, ANALYTICS AND APPLICATIONS

(Program Elective – IV)

| | |
|---|---|
| Instruction | 3L Hours per Week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Embedded Systems and Internet of Things.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Analyze Industrial IoT (IIoT) systems, Cyber-Physical Systems (CPS), and Cyber Manufacturing Systems (CMS) including their architectures, communication, and application domains.
2. Evaluate and model CPS-based manufacturing systems using modern engineering approaches, including supervisory control, data analytics, and AI techniques for smart production.
3. Design and develop intelligent industrial solutions by integrating IIoT, machine learning, big data analytics, and smart automation for real-world applications.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. An ability to independently carry out research/investigation and development work to solve practical problems in Industrial IoT and Cyber-Physical Systems.
2. An ability to write and present a substantial technical report/document related to IIoT, CPS, and smart manufacturing applications.
3. Students should be able to demonstrate a degree of mastery over Industrial IoT, CPS, and advanced manufacturing systems beyond undergraduate level.
4. Students will be able to use modern engineering tools/software to design and develop embedded, IoT-based, and intelligent industrial systems as per industry requirements.
5. Students will be able to develop self-confidence, teamwork, lifelong learning skills, and commitment towards social responsibilities in the context of smart and sustainable industrial systems.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 2 | 2 | 2 | 1 |
| **CO2** | 3 | 2 | 3 | 3 | 2 |
| **CO3** | 3 | 2 | 3 | 3 | 1 |
| **CO4** | 3 | 2 | 3 | 2 | 1 |
| **CO5** | 3 | 3 | 3 | 3 | 2 |

**UNIT – I**

**Understanding Industrial Internet of Things (IIoT):** Industrial Internet of Things and Cyber Manufacturing Systems, Application Map for Industrial Cyber Physical Systems, Cyber Physical Electronics Production.

**UNIT – II**

**Modeling of CPS and CMS:** Modeling of Cyber Physical Engineering and Manufacturing, Model based Engineering of Supervisory Controllers for Cyber Physical Systems, Evaluation Model for Assessments of Cyber Physical Production Systems.

**UNIT – III**

**Architectural Design Patterns for CMS and IIoT:** CPS-Based Manufacturing and Industry 4.0., Integration of Knowledge Base Data Base and Machine Vision, Interoperability in Smart Automation, Enhancing Resiliency in Production Facilities through CPS. Communication and Networking of IIoT.

**UNIT – IV**

**Artificial Intelligence and Data Analytics for Manufacturing:** Application of CPS in Machine Tools, Digital Production, Cyber Physical System Intelligence, Introduction to Big Data, Machine Learning and Condition Monitoring. Evaluation of Workforce and Human Machine Interaction: Worker and CPS, Strategies to Support user Intervention.

**UNIT – V**

**Introduction to Advance Manufacturing and Innovation Ecosystems:** Application of IIoT, Smart Metering, E-Health Body Area Networks, City Automation, Automotive Applications, Home Automation, Smart Cards, Plant Automation, Real Life examples of IIoT in Manufacturing Sector. Industrial IoT - Application Domains: Oil, Chemical and Pharmaceutical Industry, Applications of UAVs in Industries.

**TEXTBOOKS:**


1. Sabina Jeschke, Christian Brecher Houbing Song, Danda B. Rawat "Industrial Internet of Things Cyber Manufacturing Systems", springer, 2016.
2. Alasdair Gilchrist, "Industry 4.0: The Industrial Internet of Things", Apress, 2017


**SUGGESTED READING:**


1. The Internet of Things: Key Applications and Protocols, Olivier Hersent Actility, David Boswarthick ETSI, Omar Elloumi Alcatel-Lucent, 2nd Edition, Wiley Publications. 2012.
2. Internet of Things- From Research and Innovation to Market Deployment; By Ovidiu & Peter; River Publishers Series, 2022.

**26ECC208**

## IoT AND RTOS LAB

| | |
|---|---|
| Instruction | 2P Hours per Week |
| Duration of SEE | -- |
| SEE | -- |
| CIE | 50 Marks |
| Credits | 1 |

**PREREQUISITE:** Students should have in depth knowledge of Computer Networks and Internet of Things.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Apply the fundamentals of embedded systems by interfacing sensors and actuators using Raspberry Pi and implementing basic control programs.
2. Design and implement IoT-based applications using communication protocols such as MQTT and cloud platforms like ThingSpeak for real-time data acquisition and monitoring.
3. Analyze and implement real-time system concepts including task scheduling, multitasking, and inter-process communication using VxWorks.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Apply the knowledge of mathematics, science, and engineering fundamentals to understand embedded systems, IoT devices, and real-time operating systems.
2. Identify, formulate, and analyze problems related to sensor interfacing, communication protocols, and RTOS-based task execution.
3. Design and develop IoT-based systems using Raspberry Pi by integrating sensors, actuators, and communication protocols such as MQTT, TCP, and UDP.
4. Conduct experiments on IoT and RTOS platforms, analyze sensor data, and interpret results for efficient system performance.
5. Use modern tools and platforms such as Raspberry Pi, BeagleBone Black, cloud platforms like ThingSpeak, and RTOS like VxWorks for system design and implementation.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 2 | - | 2 |
| **CO2** | 2 | 2 | 3 | 2 | 3 |
| **CO3** | 2 | 3 | 2 | 3 | 2 |
| **CO4** | 2 | 3 | 3 | 2 | 2 |
| **CO5** | 2 | 2 | 3 | 3 | 3 |

**List of Experiments:**

**Part A: Raspberry Pi & IoT**

1. Familiarization with Raspberry Pi hardware and software installation.
2. Interfacing LED/Buzzer with Raspberry Pi and writing a program to turn ON LED for 1 second after every 2 seconds.

3. Interfacing Push Button/Digital Sensor (IR/LDR) with Raspberry Pi and writing a program to turn ON LED when push button is pressed or sensor detects.
4. Interfacing DHT11 sensor with Raspberry Pi and writing a program to display temperature and humidity readings.
5. Develop a code on Raspberry Pi to upload and retrieve sensor data using ThingSpeak cloud.
6. Develop a code on BeagleBone Black/ Raspberry Pi to publish and subscribe sensor data using MQTT protocol.

**Part B: RTOS (VxWorks)**

7. Introduction to VxWorks and its basic functions.
8. RTOS Timer programming using VxWorks.
9. RTOS Task function programming using VxWorks.
10. Multitasking using Round Robin Scheduling.
11. Inter-Process Communication (IPC) using Message Queues.
12. Inter-Process Communication (IPC) using Semaphores.
13. Inter-Process Communication (IPC) using Mailbox.

**Note: Minimum of 10 experiments should be performed.**

**SUGGESTED READING:**


1. Practical Python Programming for IoT, *Practical Python Programming for IoT: Build Advanced IoT Projects Using Raspberry Pi 4, MQTT, RESTful APIs, WebSockets, and Python 3*, Paperback Edition, Nov. 2020.
2. Operating System Concepts, A. Silberschatz, P. B. Galvin, and G. Gagne, *Operating System Concepts*, 8th ed. Hoboken, NJ, USA: Wiley, 2018.
3. VxWorks Programmer's Guide, Wind River Systems, *VxWorks Programmer's Guide*, 2019.

**26ECC209**

## RTL SYNTHESIS, SIMULATION AND VERIFICATION LAB

| | |
|---|---|
| Instruction | 2P Hours per Week |
| Duration of SEE | -- |
| SEE | -- |
| CIE | 50 Marks |
| Credits | 1 |

**PREREQUISITE:** Digital Design and Verilog HDL programming skills.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Understand digital design and verification concepts using FSMs, BDDs, and random test generation.
2. Design digital systems like controllers, communication interfaces, and memory using Verilog.
3. Apply testing and verification methods such as ATPG and FPGA implementation.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Demonstrate the process steps required for simulation /synthesis.
2. Design and simulate various combinational and sequential circuits using HDL.
3. Develop an RTL code for various real time applications.
4. Synthesize / Simulate an RTL code for several digital designs.
5. Build and verify various digital circuits.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 1 | 1 | 3 | 1 |
| **CO2** | 2 | 1 | 1 | 3 | 1 |
| **CO3** | 2 | 1 | 1 | 3 | 1 |
| **CO4** | 2 | 1 | 1 | 3 | 1 |
| **CO5** | 2 | 1 | 1 | 3 | 1 |

**LIST OF EXPERIMENTS:**

1. Binary Decision Diagram- Verification.
2. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
3. Vending machines - Traffic Light controller, ATM, Elevator control.
4. PCI Bus & arbiter and downloading on FPGA.
5. UART/ USART implementation in Verilog.
6. Realization of single port SRAM in Verilog.
7. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.
8. FIR/IIR filter implementation in Verilog.
9. Constrained Random Verification- Generate Random test vectors with constraints.
10. ATPG (Automatic Test Pattern Generation)- Generate test patterns for fault detection.

**SUGGESTED READING:**


1. Samir Palnitkar, "Verilog HDL, a guide to digital design and synthesis", Prentice Hall Publisher : Chaukhamba Auriyantaliya, 2nd edition, Apr 2018.
2. Doug Amos, Austin Lesea, Rene Richter, "FPGA based prototyping methodology manual", Xilinx, 2011.
3. Bob Zeidman, "Designing with FPGAs & CPLDs", Publisher: CRC Press, 1st edition, December 2017.

**26ECC210**

## MINI PROJECT

| | |
|---|---|
| Instruction | 2P Hours per Week |
| Duration of SEE | -- |
| SEE | -- |
| CIE | 50 Marks |
| Credits | 1 |

**PREREQUISITE:** Ability to do literature survey, solve problems, and effectively present technical concepts.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Develop the ability to identify and formulate engineering problems for investigation.
2. Encourage students to carry out independent or group-based mini project work under faculty guidance.
3. Promote research-oriented thinking through literature survey, analysis, and solution development.

**COURSE OUTCOMES:**

**Students are able to:**

1. Identify and formulate a clear engineering problem for a mini project.
2. Develop suitable models (theoretical, numerical, or experimental) for the problem.
3. Analyze and interpret results to draw meaningful conclusions.
4. Present and document the project work in a standard technical format.
5. Demonstrate basic research and presentation skills through project work.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 1 | 3 | 3 | 1 |
| **CO2** | 3 | 1 | 3 | 3 | 1 |
| **CO3** | 3 | 1 | 3 | 3 | 2 |
| **CO4** | 3 | 2 | 3 | 3 | 1 |
| **CO5** | 3 | 3 | 2 | 2 | 2 |

**Guidelines:**

1 As part of the curriculum in the II- semester of the Program each students shall do a mini project, generally comprising about three to four weeks of prior reading, twelve weeks of active research, and finally a presentation of their work for assessment.

2 Each student will be allotted to a faculty supervisor for mentoring.

3 Mini projects should present students with an accessible challenge on which to demonstrate competence in research techniques, plus the opportunity to contribute something more original.

4 Mini projects shall have inter disciplinary / industry relevance.

5 The students can select a mathematical modeling based / Experimental investigations or Numerical modeling.

6 All the investigations are clearly stated and documented with the reasons/explanations.

7 The mini-project shall contain a clear statement of the research objectives, background of work, literature review, techniques used, prospective deliverables, detailed discussion on results, conclusions and references.

Department committee: Supervisor and two faculty coordinators

| **Guidelines for awarding marks (CIE):** | | **Max. Marks: 50** |
|---|---|---|
| **Evaluation by** | **Max. Marks** | **Evaluation Criteria / Parameter** |
| Supervisor | 20 | Progress and Review |
| | 05 | Report |
| Department Committee | 05 | Relevance of the Topic |
| | 05 | PPT Preparation |
| | 05 | Presentation |
| | 05 | Question and Answers |
| | 05 | Report Preparation |

**26ECC211**

## INDUSTRIAL INTERNSHIP / TRAINING

| | |
|---|---|
| Instruction/Demonstration/Training | 90 Hours |
| Duration of SEE | -- |
| SEE | -- |
| CIE | 50 Marks |
| Credits | 1 |

**PREREQUISITE:** Knowledge of the subject and practical hands-on experience in the relevant domain.

**COURSE OBJECTIVES:**

**This Training/Internship aims to:**

1. Exposing the students to the industrial environment.
2. Create awareness with the current industrial technological developments relevant to program domain
3. Provide opportunity to understand the social, economic and administrative considerations in organizations/rural areas

**COURSE OUTCOMES:**

**Upon completion of Training/Internship, students will be able to:**

1. Understand Engineer's responsibilities and ethics
2. Use various materials, processes, products and quality control
3. Provide innovative solutions to solve real world problems
4. Acquire knowledge in technical reports writing and presentation
5. Apply technical knowledge to real world industrial/rural situations

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | - | - | 2 | 3 |
| **CO2** | 3 | 3 | - | 2 | - |
| **CO3** | 3 | 2 | - | 3 | 1 |
| **CO4** | - | - | 3 | 1 | 2 |
| **CO5** | 3 | 3 | - | 2 | 1 |

**Training / Internship Activities:**

1. Three to Four Weeks of Industry Training/Internship or working in Consultancy or Sponsored Research projects with practical relevance in the subject and submission of completion certificate is document evidence.

2. Participation in innovation related competitions for E.g., Hackathons, Ideathons, Intra/Inter Technical Symposiums etc. and submission of certificate is document evidence.

3. Development of a new product, preparation of a business plan, or registration of a start-up shall be optional components of the internship/training. However, additional weightage in awarding credit points will be given upon submission of valid documentary evidence or certification supporting such activities.

**Implementation Guidelines:** All implementation procedures, documentation processes, and official letter formats shall be updated in accordance with the internship policy guidelines of CBIT. This includes adherence to mandatory internship requirements, defined credit framework, duration norms, institutional approvals, and submission of prescribed documents such as affidavits, reports, and evaluation records. The updated guidelines and formats will be posted on the official CBIT website for reference and compliance.

**Evaluation of Internship**: The industrial training/internship of the students will be evaluated in three stages:

a) Evaluation by the industry supervisor, with certification provided upon completion; a score or grade awarded by the industry wherever applicable.
b) Evaluation by faculty Mentor on the basis of site visit(s) or periodic communication.
c) Evaluation through seminar presentation/Viva-Voce at the Institute by the constituted committee.

**Evaluation through Seminar presentation/Viva-Voce at the institute**: Students shall give a presentation before an E*xpert Committee* constituted by college (Director, HoD/Senior faculty, mentor and faculty expert from the same department) based on his/her training/internship carried out
The evaluation will be based on the following criteria:

1 Quality of content presented
2 Proper planning for presentation
3 Effectiveness of presentation
4 Depth of knowledge and skills
5 Attendance record, daily diary, departmental reports shall be analyzed along with the internship Report.

**Monitoring / Surprise Visits**: During the internship program, the faculty mentor makes a surprise visit to the internship site, to check the student's presence physically. If the student is found to be absent without prior intimation to the concerned industry, entire training / internship may be cancelled. Students should inform through email to the faculty mentor as well as the industry supervisor at least one day prior to avail leave.

**SUGGESTED REFERENCES:**

1. AICTE Internship Policy: Guidelines and Procedures (AICTE Internship Policy.pdf.)

**CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)**

## R-26 Curriculum (with effect from AY 2027-28)

**M.E (Embedded Systems & VLSI Design)**

**SEMESTER – III**

| S.no | Course Code | Title of the Course | Scheme of Instruction | | | Scheme of Examination | | | Credits |
|---|---|---|---|---|---|---|---|---|---|
| | | | Hours per week | | | Duration of SEE in Hours | Maximum Marks | | |
| | | | L | T | P/D | | CIE | SEE | |
| **THEORY** | | | | | | | | | |
| 1 | | Program Elective-V | 3 | -- | -- | 3 | 40 | 60 | 3 |
| 2 | | Open Elective / NPTEL | 3 | -- | -- | 3 | 40 | 60 | 3 |
| **DISSERTATION** | | | | | | | | | |
| 3 | 26ECC212 | Industrial Project / Dissertation Phase I | -- | -- | 20 | -- | 100 | -- | 10 |
| **Total** | | | **6** | **--** | **20** | **6** | **180** | **120** | **16** |
| **Clock Hours Per Week: 26** | | | | | | | | | |

**L: Lecture** **D: Drawing** **CIE: Continuous Internal Evaluation**

**T: Tutorial** **P: Practical/Mini Project / Dissertation** **SEE: Semester End Examination**

**26ECE217**

## GPU ARCHITECTURE AND PROGRAMMING

(Program Elective – V)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Prior knowledge of Computer Organization and Architecture, C/C++ Programming, Data Structures, and basic concepts of Parallel Processing.

**COURSE OBJECTIVES:**

**This course aims:**

1. Understand modern GPU architectures and parallel computing concepts.
2. Develop GPU-based applications using CUDA and OpenCL.
3. Apply GPU computing for performance optimization and applications in AI, signal processing, and embedded systems.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Explain GPU architecture and SIMT execution models.
2. Develop CUDA-based parallel programs.
3. Analyze performance using optimization techniques.
4. Implement heterogeneous applications using OpenCL.
5. Apply GPU computing for real-time embedded and AI-based applications.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 1 | 2 | 1 |
| **CO2** | 2 | 3 | 3 | 2 | 2 |
| **CO3** | 2 | 3 | 2 | 3 | 2 |
| **CO4** | 2 | 2 | 3 | 3 | 2 |
| **CO5** | 2 | 2 | 3 | 2 | 3 |

**UNIT - I**

**Introduction to GPU Architecture:** Parallel Computing Basics,CPU vs GPU Architecture, SIMD vs SIMT, GPU Architecture Overview (Streaming Multiprocessors, Warps), GPU Memory Hierarchy (Global, Shared, Registers), Basic Throughput Concept, Applications in Embedded Systems.

**UNIT - II**

**CUDA Programming Fundamentals:** CUDA Programming Model, Threads, Blocks, Grids, Kernel Functions, Memory Types (Global, Shared and Constant), Synchronization Basics, Data Transfer (Host ↔ Device) and Simple Programs: Vector Addition, Matrix Multiplication.

**UNIT - III**

**GPU Performance Optimization:** Warp Execution & Divergence, Memory Coalescing, Shared Memory Optimization, Occupancy Basics, Reduction Techniques (intro only), CUDA Streams (overview only), Basic Profiling Concepts.

**UNIT - IV**

**OpenCL & Heterogeneous Computing:** OpenCL Platform Model, Execution Model, Memory Model, Kernel Programming Basics, Work-items & Work-groups,CUDA vs OpenCL (comparison).

**UNIT - V**

**Applications & Recent Trends:** GPU in Embedded Systems, Image & Signal Processing (basic kernels), Introduction to GPU in AI (no deep DL math), Edge AI & Embedded GPU Platforms, Overview of Tensor Cores, Discussion of recent GPU architectures (e.g., NVIDIA Ampere/Hopper) and research trends. (brief survey).

**TEXT BOOKS:**


1. Wen-mei W. Hwu, David B. Kirk and Izzat El Hajj, *Programming Massively Parallel Processors: A Hands-on Approach*, 4th Edition, Morgan Kaufmann, 2022.
2. Gerassimos Barlas, *Multicore and GPU Programming: An Integrated Approach*, 2nd Edition, Elsevier, 2022.
3. Richard Ansorge, *Programming in Parallel with CUDA: A Practical Guide*, Cambridge University Press, 2022.


**SUGGESTED READING:**


1. Paulo Motta, *GPU Programming with C++ and CUDA: Uncover Effective Techniques for Writing Efficient GPU-Parallel C++ Applications*, Packt Publishing, 2025.
2. Gareth Morgan Thomas, *Advanced CUDA Programming: High-Performance Computing with GPUs*, Independently Published, 2025


**NPTEL Course Link**

GPU Architectures and Programming – NPTEL:
https://onlinecourses.nptel.ac.in/e-learning/preview/noc23_cs61

**26ECE217**

# AUTOMOTIVE ELECTRONICS

(Program Elective – V)

| | |
|---|---|
| Instruction | 3 L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Basic knowledge of electronics, embedded systems, and automotive fundamentals.

**COURSE OBJECTIVES:**

**The students will be able to:**

1. Understand automotive electronic systems, vehicle architecture, and embedded components.
2. Study sensors, actuators, and communication protocols used in modern vehicles.
3. Learn ADAS, electric vehicles, safety systems, and design automotive embedded solutions.

**COURSE OUTCOMES:**

**After successful completion of the course, students will be able to:**

1. Understand the architecture and operation of automotive electronic systems.
2. Analyze automotive sensors, actuators, and electronic control units (ECUs).
3. Apply automotive communication protocols such as CAN, LIN, FlexRay, and Ethernet.
4. Evaluate safety, reliability, and security aspects in automotive electronics.
5. Design embedded solutions for automotive and electric vehicle applications.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 1 | 3 | 2 | 1 |
| **CO2** | 2 | 1 | 3 | 3 | 1 |
| **CO3** | 2 | 2 | 3 | 3 | 1 |
| **CO4** | 3 | 2 | 3 | 2 | 2 |
| **CO5** | 3 | 2 | 3 | 3 | 2 |

**UNIT – I**

**Introduction to Automotive Electronics:** Introduction to Automotive Electronics: Evolution of automotive electronics, Automotive system architecture, Electronic Control Units (ECUs), Vehicle electrical systems and power distribution, Automotive standards and regulations, Overview of embedded systems in automobiles.

**UNIT – II**

**Sensors and Actuators in Automobiles:** Automotive sensors: temperature, pressure, speed, position, oxygen, accelerometer, gyroscope.

Signal conditioning circuits, Actuators: solenoids, relays, motors, injectors, Engine management systems, Transmission control systems, Body electronics and comfort systems.

**UNIT – III**

**Automotive Communication Networks:** In-vehicle networking concepts, CAN protocol and applications, LIN, FlexRay, MOST, and Automotive Ethernet, Diagnostics and OBD-II systems, Vehicle-to-Vehicle (V2V) and Vehicle-to-Infrastructure (V2I) communication, Cybersecurity in automotive communication.

**UNIT – IV**

**Automotive Safety and Advanced Systems:** Functional safety and ISO 26262, Anti-lock braking systems (ABS), Airbag systems and traction control, Advanced Driver Assistance Systems (ADAS), Autonomous vehicle concepts, Reliability and fault-tolerant design.

**UNIT – V**

**Electric and Hybrid Vehicle Electronics:** Architecture of electric and hybrid electric vehicles, Battery Management Systems (BMS), Electric drives and motor control, Power electronics in EVs, Charging systems and energy management, Future trends in automotive electronics.

**TEXT BOOKS:**


1. William B. Ribbens, *Understanding Automotive Electronics*, Elsevier, 8th Edition, 2017.
2. Ronald K. Jurgen, *Automotive Electronics Handbook*, McGraw-Hill Education, 2nd Edition, 1999.
3. Robert Bosch GmbH, *Bosch Automotive Handbook*, Wiley, 10th Edition, 2018.


**SUGGESTED READING:**


1. Konrad Reif, *Automotive Mechatronics: Automotive Networking, Driving Stability Systems, Electronics*, Springer, 2nd Edition, 2015.
2. Nicolas Navet and Francoise Simonot-Lion, *Automotive Embedded Systems Handbook*, CRC Press, 1st Edition, 2008.

**26ECE219**

**CMOS PLL**

(Program Elective – V)

| | |
|---|---|
| Instruction | 3 L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Basic knowledge of analog electronics, feedback systems, and communication fundamentals.

**COURSE OBJECTIVES:**

**The students will be able to:**

1. Develop an understanding of various types of Oscillators and their application.
2. Develop analytical skills to analyse various Phase locked loops
3. Develop design exploration of various PLL architectures and selection of appropriate architecture for given application.

**COURSE OUTCOMES:**

**After successful completion of the course, students will be able to:**

1. Understand the fundamentals and operating principles of VCOs.
2. Analyze and design CMOS PLL building blocks such as Phase Frequency Detector (PFD), Charge Pump, Loop Filter, Voltage Controlled Oscillator (VCO), and Frequency Divider.
3. Study linear and nonlinear behavior, stability, noise, and jitter performance of PLL systems.
4. Design and simulate CMOS PLL architectures for communication and clock generation applications.
5. Understand the working of All Digital PLLs.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 2 | 1 | 2 |
| **CO2** | 3 | 3 | 1 | 3 | 1 |
| **CO3** | 3 | 3 | 3 | 2 | 2 |
| **CO4** | 3 | 3 | 3 | 3 | 2 |
| **CO5** | 3 | 3 | 3 | 3 | 2 |

**UNIT-I**

**Oscillators:** Basic Concepts, Oscillatory feedback systems, Ring OScillator, LC Oscillators, Voltage Controlled Oscillators, Oscillator Jitter and Phase Noise. Phaae noise in Ring Oscillator.

**UNIT-II**

**Introduction to PLLs:**

Introduction to PLLs, Basic principles of operation, Linear PLL model, Phase detector characteristics, Lock range and capture range, PLL transfer function – Applications of PLLs in communication and clock generation systems..

**Charge Pump PLLs:** Type-I vs Type-II PLLs, Phase detector and Phase Frequency Detector (PFD), characteristics of PFD, Charge pump.

**UNIT-III**

**Analysis of PLL:** Linear analysis of Charge Pump PLL, PLL acquisition behavior, Stability analysis of CP PLL, Loop Filters, Loop bandwidth optimization.

**UNIT-IV**

**PLL synthesizers:** Frequency synthesis techniques, Integer-N and Fractional-N PLLs, Spur mechanisms. Frequency dividers and prescalers, CMOS implementation of Frequency Dividers.

**UNIT-V**

**Noise and ADPLL:** Phase noise sources in PLLs, Jitter analysis, Noise transfer functions, Delay Locked Loop (DLL) , All Digital PLL (ADPLL).

**TEXT BOOKS:**

1. Behzad Razavi, *Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level*, Cambridge University Press, 2020.
2. Roland E. Best, *Phase-Locked Loops: Design, Simulation and Applications*, McGraw Hill,2003.

**SUGGESTED READING:**

1. Dean Banerjee, *PLL Performance, Simulation and Design*, National Semiconductor, 2006.
2. Floyd M. Gardner, *Phaselock Techniques*, Wiley-Interscience, 2005.
3. William F. Egan, *Frequency Synthesis by Phase Lock*, Wiley, 2000.

**26ECE220**

## 3D INTERCONNECTS

(Program Elective – V)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PREREQUISITE:** Fundamentals of VLSI Design, Digital Integrated Circuits, Network Theory, Transmission Lines, and basic knowledge of VLSI CAD tools.

**COURSE OBJECTIVES:**

**This course aims:**

1. To provide a strong understanding of VLSI interconnect modeling, delay analysis, and scaling effects in modern integrated circuits.
2. To analyze electrical phenomena in interconnects such as resistance, inductance, skin effect, electromigration, and crosstalk, along with their mitigation techniques.
3. To develop knowledge of advanced 3D interconnect technologies, packaging methods, and design considerations for high-performance and reliable 3D integrated circuits.

**COURSE OUTCOMES:**

**After successful completion of the course, students will be able to:**

1. Explain VLSI interconnect concepts, distributed RC models, scaling effects, and analyze delay characteristics using suitable interconnect models.
2. Analyze inductive effects in interconnects using RLC models, transmission line equations, and simulation techniques.
3. Evaluate high-frequency effects such as skin effect, power dissipation, and electro migration and propose suitable mitigation methods.
4. Analyze crosstalk effects and estimate interconnect parameters through extraction and simulation techniques.
5. Apply concepts of 3D integration, TSVs, silicon interposers, packaging technologies, and thermal management techniques in the design of advanced 3D IC systems.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 2 | 1 | 2 | 2 |
| **CO2** | 3 | 3 | 2 | 3 | 2 |
| **CO3** | 2 | 3 | 2 | 3 | 2 |
| **CO4** | 3 | 3 | 2 | 3 | 3 |
| **CO5** | 3 | 2 | 3 | 2 | 3 |

**UNIT–I**

**Introduction to VLSI Interconnects:**Introduction to VLSI interconnects, Distributed RC interconnect model,Elmore delay in interconnects,Scaling effects in interconnects,Simulation and delay mitigation in RC interconnects

**UNIT–II**

**Inductive Effects in Interconnects:** Inductive effects in interconnects Distributed RLC interconnect model, Transmission line equations, Conditions for considering inductive effects, Equivalent Elmore model for RLC interconnects, Two-pole model of RLC interconnects using ABCD parameters, RLC interconnect simulation

**UNIT–III**

**Skin Effect and Electromigration:** Origin of skin effect,Effective resistance at high frequencies,Power dissipation due to interconnects,Electromigration in interconnects,Techniques to mitigate electromigration

**UNIT–IV**

**Crosstalk and Interconnect Extraction:**Capacitive coupling in interconnects,Crosstalk effects in identical interconnects,Crosstalk mitigation techniques, Analysis and simulation of coupled interconnects,Extraction of capacitance,Extraction of inductance,Estimation of interconnect parameters using S-parameters

**UNIT–V**

**3D Technology and Packaging Techniques:**Silicon interposer technology,Through Silicon Vias (TSVs),Hybrid packaging techniques,Silicon-less interconnect technology,3D integrated architectures,Physical design and thermal management techniques for 3D ICs,Case study: Clock distribution networks in 3D ICs,Trends in packaging and future interconnect technologies

**TEXT BOOKS:**


1. **Vasilis F. Pavlidis, Eby G. Friedman** *Three-Dimensional Integrated Circuit Design* Morgan Kaufmann, Elsevier, 2009.
2. **Ashok K. Goel:** *High-Speed VLSI Interconnects,*Wiley India, 2007.
3. **Y. S. Diamand,** *Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications* 2009.
4. **Rao R. Tummala** *Fundamentals of Microsystems Packaging,*McGraw-Hill, 2001.


**REFERENCE BOOKS:**


1. **John H. Lau:** *Through-Silicon Vias for 3D Integration* McGraw-Hill, 2012.
2. **Antonis Papanikolaou, Dimitrios Soudris, Riko Radojcic,***Three Dimensional System Integration: IC Stacking Process and Design* Springer, 2011.
3. **Yuan Xie, Jason Cong, Sachin Sapatnekar,** *Three-Dimensional Integrated Circuit Design: EDA, Design and Microarchitectures* Springer
4. **H. S. Philip Wong, Deji Akinwande ,** *Carbon Nanotube and Graphene Device Physics* For emerging interconnect technologies.

**26ECC212**

## INDUSTRIAL PROJECT / DISSERTATION PHASE I

| | |
|---|---|
| Instruction | 20 P Hours per Week |
| Duration of SEE | -- |
| SEE | -- |
| CIE | 100 Marks |
| Credits | 10 |

**PREREQUISITE:** Capable of carrying out suitable literature survey and accomplish/execute a software/hardware based project in Embedded, VLSI and allied areas.

**COURSE OBJECTIVES:**

**This course aims to:**

1. The 'Industrial project/Dissertation Phase 1(Project work) will preferably be a problem with research potential and should involve scientific research, design, generation/collection and analysis of data, determining solution and must preferably bring out the student contribution(s).
2. Expose and learn the required simulation software/experimental techniques.
3. Carry out the work in a research environment or in an industrial environment.

**COURSE OUTCOMES:**

**After successful completion of the course, students will be able to:**

1. Ability to synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem.
2. Learn the required software/ computational/analytical tools for implementations.
3. Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design.
4. Ability to present the findings of their technical solution in a written report.
5. Presenting the work in International/ National conference or reputed journals.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 3 | 3 | 1 |
| **CO2** | 3 | 3 | 3 | 3 | 2 |
| **CO3** | 3 | 3 | 3 | 3 | 2 |
| **CO4** | 3 | 3 | 2 | 3 | 1 |
| **CO5** | 2 | 2 | 2 | 3 | 2 |

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have the following.

- Relevance to social needs of society.
- Relevance to value addition to existing facilities in the institute.
- Relevance to industry need.
- Problems of national importance.
- Research and development in various domain.

The student should complete the following:

- Literature survey Problem Definition.
- Motivation for study and Objectives.
- Preliminary design / feasibility / modular approaches.
- Implementation and Verification.

- Report and presentation.

**As per the AICTE and Institute directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e., Phase – I and Phase – II.**

**Guidelines for Dissertation Phase – I:**

- The dissertation may be carried out preferably in-house i.e., departments laboratories and centers OR in industry allotted through departments T & P coordinator.

- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Embedded and VLSI domains. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.

- Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.

- Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.

- Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.

| Guidelines for awarding Marks in CIE: | | Max. Marks: 100 |
|---|---|---|
| **Evaluation by** | **Max. Marks** | **Evaluation Criteria / Parameter** |
| Supervisor | 30 | Project Status / Review(s) |
| | 20 | Report |
| Departmental Review Committee | 10 | Relevance of the Topic |
| | 10 | PPT Preparation(s) |
| | 10 | Presentation(s) |
| | 10 | Question and Answers |
| | 10 | Report Preparation |

**Note:** Departmental Review committee has to assess the progress of the student for every two weeks.

**CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)**

## R-26 Curriculum (with effect from AY 2027-28)

**M.E (Embedded Systems & VLSI Design)**

**SEMESTER – IV**

| S.no | Course Code | Title of the Course | Scheme of Instruction | | | Scheme of Examination | | | Credits |
|---|---|---|---|---|---|---|---|---|---|
| | | | Hours per week | | | Duration of SEE in Hours | Maximum Marks | | |
| | | | L | T | P/D | | CIE | SEE | |
| **DISSERTATION** | | | | | | | | | |
| 1 | 26ECC213 | Industrial Project / Dissertation Phase II | -- | -- | 32 | Viva-Voce | 100 | 100 | 16 |
| **Total** | | | -- | -- | **32** | -- | **100** | **100** | **16** |
| **Clock Hours Per Week: 32** | | | | | | | | | |

**L: Lecture** **D: Drawing** **CIE: Continuous Internal Evaluation**

**T: Tutorial** **P: Practical/Mini Project /Dissertation** **SEE: Semester End Examination**

**26ECC213**

## INDUSTRIAL PROJECT / DISSERTATION PHASE II

| | |
|---|---|
| Instruction | 32 P Hours per Week |
| Duration of SEE | Viva - Voce |
| SEE | 100 Marks |
| CIE | 100 Marks |
| Credits | 16 |

**PREREQUISITE:** Should have completed literature survey and defined problem statement with a brief idea of the methodology, as a part of Industrial Project/ Dissertation Phase-I.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Industrial Project / Dissertation Phase 2 is the continuation of Industrial Project / Dissertation Phase 1.
2. Implementation of Project objectives.
3. Presentation of periodic reviews of the objectives and preparing of Dissertation in a prescribed format.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Ability to synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem.
2. Learn the required software/ computational/analytical tools for implementations.
3. Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design.
4. Ability to present the findings of their technical solution in a written report.
5. Presenting the work in International/ National conference or reputed journals.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 3 | 3 | 2 | 3 | 2 |
| **CO2** | 3 | 3 | 3 | 3 | 2 |
| **CO3** | 3 | 3 | 3 | 3 | 2 |
| **CO4** | 3 | 3 | 3 | 3 | 2 |
| **CO5** | 3 | 2 | 2 | 2 | 2 |

As per the AICTE and Institute directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I. and Phase – II.

**Syllabus Contents:**

- The dissertation may be carried out preferably in-house i.e. departments laboratories and centers OR in industry allotted through departments T & P coordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Embedded and VLSI domains.
- In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.

**Guidelines for Dissertation Phase – II:**
The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be based on:

- Experimental verification / Proof of concept.
- Design, fabrication, testing of Communication System.
- The viva-voce examination will be based on the above report and work.

During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.

- Phase – II deliverables: A dissertation report as per the specified format, developed system in the form of hardware and/or software, A record of continuous progress.
- Phase – II evaluation: Guide along with appointed external examiner shall assess the progress / performance of the student based on report, presentation and Q & A.
- In case of unsatisfactory performance, committee may recommend for extension or repeating the work.

| Guidelines for awarding marks in CIE: Max. Marks: 100 | | |
|---|---|---|
| **Evaluation by** | **Max. Marks** | **Evaluation Criteria / Parameter** |
| Departmental Review Committee | 05 | Review 1 |
| | 10 | Review 2 |
| | 10 | Review 3 |
| | 15 | Final presentation with the draft copy of the report |
| | 10 | Submission of the report in a standard format |
| Supervisor | 10 | Regularity and Punctuality |
| | 10 | Work Progress |
| | 10 | Quality of the work which may lead to publications |
| | 10 | Analytical / Programming / Experimental Skills |
| | 10 | Report preparation in a standard format |

| Guidelines for awarding marks in SEE: Max. Marks: 100 | | |
|---|---|---|
| **Evaluation by** | **Max. Marks** | **Evaluation Criteria / Parameter** |
| External and Internal Examiner(s) together | 20 | Power Point Presentation |
| | 40 | Quality of thesis and evaluation |
| | 20 | Quality of the project<br>• Innovations<br>• Applications<br>• Live Research Projects<br>• Scope for future study<br>• Application to society |
| | 20 | Viva-Voce |

**Note:** Departmental Review committee has to assess the progress of the student for every two weeks

**26CEA101**

**DISASTER MITIGATION AND MANAGEMENT**
**(Audit Course)**

| | |
|---|---|
| Instruction | 2L Hours per Week |
| Duration of SEE | 2 Hours |
| SEE | 50 Marks |
| CIE | - |
| Credits | - |

## COURSE OBJECTIVES:

**To enable the student:**

1. To equip the students with the basic knowledge of hazards, disasters, risks and vulnerabilities, including natural, climatic and human-induced factors and associated impacts
2. To impart knowledge in students about the nature, causes, consequences and mitigation measures of the various natural disasters
3. To enable the students to understand risks, vulnerabilities and human errors associated with human-induced disasters
4. To enable the students to understand and assimilate the impacts of any disaster on the affected area, depending on its position/ location, environmental conditions, demographic, etc.
5. To equip the students with the knowledge of the chronological phases in a disaster management cycle and to create awareness about the disaster management framework and legislations in the context of national and global conventions

## COURSE OUTCOMES:

**At the end of the course, students will be able to:**

1. Ability to analyse and critically examine existing programs in disaster management regarding vulnerability, risk and capacity at different levels.
2. Ability to understand and choose the appropriate activities and tools, and set up priorities to build a coherent and adapted disaster management plan.
3. Ability to understand various mechanisms and consequences of human-induced disasters for the participatory role of engineers in disaster management.
4. To understand the impact on various elements affected by the disaster and to suggest and apply appropriate measures for the same.
5. Develop an awareness of the chronological phases of disaster preparedness, response and relief operations for formulating effective disaster management plans and the ability to understand various participatory approaches/strategies and their application in disaster management.

## CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 3 | 2 | 1 | 1 |
| **CO2** | 3 | 3 | 2 | 2 | 1 |
| **CO3** | 2 | 3 | 3 | 2 | 1 |
| **CO4** | 3 | 3 | 2 | 3 | 1 |
| **CO5** | 3 | 2 | 2 | 3 | 1 |

**UNIT- I**

**Introduction:** Basic definitions- Hazard, Disaster, Vulnerability, Risk, Resilience, Mitigation, Management; classification of types of disaster-Natural and manmade; International Decade for natural disaster reduction (IDNDR); International strategy for disaster reduction (ISDR), National disaster management authority (NDMA).

**UNIT- II**

**Natural Disasters**: Hydro meteorological disasters: Causes, Early warning systems- monitoring and management, structural and non-structural measures for floods, drought and Tropical cyclones; Geographical based disasters: Tsunami generation, causes, zoning, Early warning systems-monitoring and management, structural and non-structural mitigation measures for earthquakes, tsunami, landslides, avalanches and forest fires. Case studies related to various hydro-meteorological and geographical based disasters.

**UNIT- III**

**Human induced hazards:** Chemical disaster- Causes, impacts and mitigation measures for chemical accidents, Risks and control measures in a chemical industry, chemical disaster management; Case studies related to various chemical industrial hazards eg.: Bhopal gas tragedy; Management of chemical terrorism disasters and biological disasters; Radiological Emergencies and case studies; Case studies related to major power break downs, fire accidents, traffic accidents, oil spills and stampedes, disasters due to double cellar construction in multistoried buildings.

**UNIT- IV**

**Disaster Impacts:** Disaster impacts- environmental, physical, social, ecological, economic, political, etc.; health, psycho-social issues; demographic aspects- gender, age, special needs; hazard locations; global and national disaster trends; climate change and urban disasters.

**UNIT- V**

**Concept of Disaster** Policies and legislation for disaster risk reduction

**Management:** Disaster management cycle – its phases; prevention, mitigation, preparedness, relief and recovery; risk analysis, vulnerability and capacity assessment; post-disaster environmental response water, sanitation, food safety, waste management, disease control; Roles and responsibilities of government, community, local in situations, NGOs and other stakeholders;, DRR programmers in India and the activities of National Disaster Management Authority.

**TEXT BOOKS:**

1. Pradeep Sahni*," Disaster Risk Reduction in South Asia*", Prentice Hall, 2003.
2. B. K. Singh,*" Handbook of Disaster Management*: *techniques &Guidelines*", Rajat Publication, 2008.
*3.* Ministry of Home Affairs". *Government of India, "National disaster management plan, Part I and II",*
4. K. K.Ghosh," *Disaster Management",* APH Publishing Corporation, 2006.

**SUGGESTED READING:**

1. http://www.indiaenvironmentportal.org.in/files/file/disaster_management_india1.pdf
2. http://www.ndmindia.nic.in/ (National Disaster management in India, Ministry of Home Affairs)
3. Hazards, Disasters and your community: A booklet for students and the community, Ministry of home affairs.

**26EGA101**

# ENGLISH FOR RESEARCH PAPER WRITING

**(Audit Course)**

| | |
|---|---|
| Instruction | 2L Hours per Week |
| Duration of SEE | 2 Hours |
| SEE | 50 Marks |
| CIE | - |
| Credits | - |

**PREREQUISITE**: Writing to express on science and technological concepts with good taste for research and development.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Motivate learners for academic writing and thus encourage them for continuous professional updating and up-gradation.
2. Facilitate a practical understanding of the multiple purposes of Writing Research Papers and help them infer the benefits and limitations of research in science and technology.
3. Brainstorm and develop the content, formulating a structure and illustrating the format of writing a research paper.
4. Survey and select a theme/topic for a thorough reading and to writing a research paper.
5. Understand to implement the intricacies of writing and publishing a research paper.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Improve work performance and efficiency. Illustrate the nuances of research paper writing and draw conclusions on professional usefulness.
2. Classify different types of research papers and organize the format and citation of sources.
3. Explore various formats of APA, MLA and IEEE and set up for writing a research paper.
4. Draft paragraphs and write theme based thesis statements in a scientific manner.
5. Develop an original research paper while acquiring the knowledge of how and where to publish their papers.

## CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 1 | 2 | 1 | 1 | 1 |
| **CO2** | 1 | 1 | 1 | 1 | 1 |
| **CO3** | 1 | 2 | 2 | 1 | 1 |
| **CO4** | 1 | 2 | 1 | 1 | 1 |
| **CO5** | 2 | 3 | 1 | 1 | 1 |

**UNIT - I**

Academic Writing: Meaning & Definition of a research paper; Purpose of a research paper - Scope, Benefits, Limitations and outcomes for professional development, An introduction to methods and Approaches of Research.

**UNIT - II**

Research Paper Format: Title - Abstract - Introduction - Discussion - Findings - Conclusion - Style of Indentation - Font size/Font types - Indexing - Citation of sources.

**UNIT - III**
Process of Writing a research paper, Writing to Draft a Format, Develop content, Adapting, Reviewing, Paraphrasing& Plagiarism Checks.

**UNIT - IV**
Choosing a topic - Thesis Statement - Outline - Organizing notes - Language of Research - Word order, Paragraphs - Writing first draft-Revising/Editing - The final draft and proof reading. Understanding APA, MLA, IEEE formats.

**UNIT - V**
Research Paper Publication Reputed Journals –Paid, Free and peer reviewed journals, National/International - ISSN No, No. of volumes, Scopus Index/UGC Journals. Getting Papers Published.

**TEXT BOOKS:**


1. Kothari, C. R. and Gaurav, Garg, Research Methodology Methods and Techniques", 4thEdition, New Age International Publishers, New Delhi, 2019.
2. Ellison, Carroll. "Writing Research Papers", McGraw Hill's Concise Guide, 2010.
3. Lipson, Charles. "Cite Right: A Quick Guide to Citation Styles-- MLA, APA, Chicago, the Sciences, Professions, and More", 2nd Edition,. University of Chicago Press. Chicago, 2018.


**SUGGESTED READING:**


1. Day, Robert A. "How to Write and Publish a Scientific Paper", Cambridge University Press, 2006
2. Girden, E. R. "MLA Hand book for writers of Research Papers", 7th Edition, East West Press Pvt. Ltd, New Delhi, 2009
3. Bailey, Stephen. "Academic Writing: A Handbook for International Students", Routledge, 2018.


**ONLINE RESOURCES:**

1. https://onlin://onlinecourses.nptel.ac.in/noc 18_mg13/preview
2. https://nptel.ac.in/courses/121/106/121106007/
3. https://www.classcentral.com/course/swayam-introduction-to-research-5221

**WRITING TOOLS:**

1. https://owl.purdue.edu/owl_exercises/index.html - The Owl writing lab
2. https://www.turnitin.com/login_page.asp?lang=en_us – Turn tin software

**26EGA102**

# CONSTITUTION OF INDIA

**(Audit Course)**

| | |
|---|---|
| Instruction | 2L Hours per Week |
| Duration of SEE | 2 Hours |
| SEE | 50 Marks |
| CIE | - |
| Credits | - |

**PREREQUISITE**: Knowledge on basics of the Constitution and the Government.

**COURSE OBJECTIVES**:

**This course aims to:**

1. The history of Indian Constitution and its role in the Indian democracy.
2. Address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. Have knowledge of the various Organs of Governance and Local Administration.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Understand the making of the Indian Constitution and its features.
2. Understand the Rights of equality, the Right of freedom and the Right to constitutional remedies.
3. Have an insight into various Organs of Governance - composition and functions.
4. Understand powers and functions of Municipalities, Panchayats and Co-operative Societies.
5. Understand Electoral Process, special provisions.

## CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 1 | 1 | - | 1 | 1 |
| **CO2** | 1 | 1 | - | 1 | 1 |
| **CO3** | 1 | 1 | - | 1 | 1 |
| **CO4** | 1 | 1 | - | 1 | 1 |
| **CO5** | 1 | 1 | - | 1 | 1 |

**UNIT-I**

**History of making of the Indian constitutions** - History, Drafting Committee (Composition & Working).

**Philosophy of the Indian Constitution**: Preamble, Salient Features.

**UNIT-II**

**Contours of Constitutional Rights and Duties -** Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights,

Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

**UNIT-III**

**Organs of Governance -** Parliament : Composition, Qualifications, Powers and Functions

Union executives : President, Governor, Council of Ministers, Judiciary, appointment and transfer of judges,qualifications, powers and functions.

**UNIT-IV**

**Local Administration -** District's Administration head: Role and importance.

**Municipalities:** Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Panchayati Raj: Introduction, PRI: ZillaPanchayat, Elected Officials and their roles, CEO ZillaPanchayat: positions and role.

**Block level:** Organizational Hierarchy (Different departments) Village level: role of elected and appointed officials. Importance of grass root democracy.

**UNIT-V**

**Election commission**: Role and functioning, Chief Election Commissioner and Election Commissioners, State Election Commission :Role and functioning. Institute and Bodies for the welfare of SC/ST/OBC and women**.**

**TEXT BOOKS:**


1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Busi, S. N., Dr. B. R. Ambedkar, Framing of Indian Constitution'', 1st Edition, Ava Publishers, New Delhi, 2015.
3. Jain, M. P., "Indian Constitution Law", 7th Edition, Lexis Nexis, New Delhi, 2014.
4. Basu, D.D. "Introduction to the Constitution of India", Lexis Nexis, New Delhi., 2015.


**SUGGESTED READING:**


1. Bhargava, Rajeev. (ed), "Politics and Ethics of the Indian Constitution", OUP, 2008.
2. NCERT, Indian Constitution at Work, 1st Edition, Government of India, New Delhi 2006, reprinted in 2022.
3. Ravindra Sastry, V. (ed.), Indian Government & Politics, 2nd edition, Telugu Akademy, 2018.


**ONLINE RESOURCES:**

1. http://www.nptel.ac.in/courses/103107084/Script.pdf

**26ADA101**

# PEDAGOGY STUDIES

**(Audit Course)**

| | |
|---|---|
| Instruction | 2L Hours per Week |
| Duration of SEE | 2 Hours |
| SEE | 50 Marks |
| CIE | - |
| Credits | - |

**COURSE OBJECTIVES:**

**This course aims to:**

1. Present the basic concepts of design and policies of pedagogy studies.
2. Provide understanding of the abilities and dispositions with regard to teaching techniques, curriculum design and assessment practices.
3. Familiarize various theories of learning and their connection to teaching practice.
4. Create awareness about the practices followed by DFID, other agencies and other researchers.
5. Provide understanding of critical evidence gaps that guides the professional development.

**COURSE OUTCOMES:**

**Upon completing this course, students will be able to:**

1. Illustrate the pedagogical practices followed by teachers in developing countries both in formal and informal classrooms.
2. Examine the effectiveness of pedagogical practices.
3. Understand the concept, characteristics and types of educational research and perspectives of research.
4. Describe the role of classroom practices, curriculum and barriers to learning.
5. Understand Research gaps and learn the future directions.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 1 | 1 | 1 | 2 | 2 |
| **CO2** | 1 | 1 | 1 | 2 | 2 |
| **CO3** | 2 | 2 | 2 | 2 | 2 |
| **CO4** | 1 | 1 | 1 | 2 | 2 |
| **CO5** | 2 | 2 | 2 | 2 | 2 |

**UNIT - I**

**Introduction and Methodology:** Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education, Conceptual framework, Research questions, Overview of methodology and Searching.

**UNIT - II**

**Thematic Overview:** Pedagogical practices followed by teachers in formal and informal classrooms in developing countries, Curriculum, Teacher education.

**UNIT - III**

**Evidence on the Effectiveness of Pedagogical Practices:** Methodology for the in depth stage: quality assessment of included studies - How can teacher education (curriculum and Practicum) and the school curriculum and guidance material best support effective pedagogy? - Theory of change - Strength and nature of the body of evidence for effective pedagogical practices - Pedagogic theory and pedagogical approaches - Teachers' attitudes and beliefs and pedagogic strategies.

**UNIT - IV**

**Professional Development:** alignment with classroom practices and follow up support, Support from the head teacher and the community, Curriculum and assessment.

**Barriers to learning:** Limited resources and large class sizes.

**UNIT - V**

**Research Gaps and Future Directions:** Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

**TEXT BOOKS:**


1. Ackers J, Hardman F, "Classroom Interaction in Kenyan Primary Schools, Compare", 31 (2): 245 – 261, 2001.
2. Agarwal M, "Curricular Reform in Schools: The importance of evaluation", Journal of Curriculum Studies, 36 (3): 361 – 379, 2004.


**SUGGESTED READING:**


1. Akyeampong K, "Teacher Training in Ghana – does it count? Multisite teacher education research project (MUSTER)", Country Report 1.London: DFID, 2003.
2. Akyeampong K, Lussier K, Pryor J, Westbrook J, "Improving teaching and learning of Basic Maths and Reading in Africa: Does teacher Preparation count?, International Journal Educational Development, 33 (3): 272- 282, 2013.
3. Alexander R J, "Culture and Pedagogy: International Comparisons in Primary Education", Oxford and Boston: Blackwell, 2001.
4. Chavan M, "Read India: A mass scale, rapid, 'learning to read' campaign", 2003.


**WEB RESOURCES:**

1. https://onlinecourses.nptel.ac.in/noc17_ge03/preview
2. www.pratham.org/images/resources%20working%20paper%202.pdf.

**26EGA104**

## PERSONALITY DEVELOPMENT THROUGH LIFE'S ENLIGHTENMENT SKILLS

**(Audit Course)**

| | |
|---|---|
| Instruction | 2L Hours per Week |
| Duration of SEE | 2 Hours |
| SEE | 50 Marks |
| CIE | - |
| Credits | - |

**PREREQUISITE**: Awareness on Personality Development.

**COURSE OBJECTIVES**:

**This course aims to:**

1. Learn to achieve the highest goal happily.
2. Become a person with stable mind, pleasing personality and determination.
3. Awake wisdom among themselves.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Develop their personality and achieve their highest goal of life.
2. Lead the nation and mankind to peace and prosperity.
3. Practice emotional self regulation.
4. Develop a positive approach to work and duties.
5. Develop a versatile personality.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 1 | 1 | - | 1 | 1 |
| **CO2** | 1 | 1 | - | 1 | 1 |
| **CO3** | 1 | 1 | - | 1 | 1 |
| **CO4** | 1 | 1 | - | 1 | 1 |
| **CO5** | 1 | 1 | - | 1 | 1 |

**UNIT - I**

**Neetisatakam – Holistic development of personality** - Verses 19, 20, 21, 22 (Wisdom) - Verses 29, 31, 32 (Pride and Heroism) - Verses 26,28,63,65 (Virtue)

**UNIT - II**

**Neetisatakam – Holistic development of personality (cont'd**) - Verses 52, 53, 59 (dont's) - Verses 71,73,75& 78 (do's) - Approach to day to day works and duties.

**UNIT - III**

**Introduction to Bhagavadgeetha for Personality Development – Shrimad Bhagawad Geeta**: Chapter 2–Verses 41, 47, 48 - Chapter 3 – Verses 13,21,27,35 - Chapter 6 – Verses 5,13,17,23,35 - Chapter 18 –Verses 45, 46, 48 Chapter – 6: Verses 5, 13, 17, 23, 35; Chapter – 18: Verses 45, 46, 48

**UNIT - IV**

**Statements of basic knowledge – Shrimad Bhagawad Geeta**: Chapter 2- Verses 56, 62,68 - Chapter 12 – Verses 13, 14, 15, 16, 17, 18 - Personality of Role model from Shrimad Bhagawat Geeta.

**UNIT - V**

**Role of Bhagawadgeeta in the present scenario -** Chapter 2 – Verses 17 - Chapter 3 – Verses 36, 37, 42 - Chapter 4 – Verses 18, 38, 39 - Chapter 18 – Verses 37, 38, 63.

**TEXT BOOKS:**


1. Gopinath, P., "Bhartrihari's Three Satakam (Niti-sringar-vairagya)", Rashtriya Sanskrit Sansthanam, New Delhi, 2018.
2. Swarupananda, Swami, "Srimad Bhagavad Geeta", Advaita Ashram (Publication Dept), Kolkata, 2017.


**ONLINE RESOURCES:**

1. http://nptel.ac.in/downloads/109104115/

**26EEA101**

## SANSKRIT FOR COMPUTATIONAL THINKING & ENGINEERING APPLICATIONS

**(Audit Course)**

| | |
|---|---|
| Instruction | 2L Hours per Week |
| Duration of SEE | 2 Hours |
| SEE | 50 Marks |
| CIE | - |
| Credits | - |

## COURSE OBJECTIVES:

**This course aims to:**

1. To introduce Sanskrit as a structured language useful for logical thinking and algorithm design.
2. To connect Sanskrit concepts with modern engineering domains (AI, circuits, structures, systems).
3. To develop computational and analytical skills using Sanskrit-based principles.
4. To enable students to explore interdisciplinary applications for research and innovation.

## COURSE OUTCOMES:

**After completion, students will be able to:**

1. Apply structured Sanskrit rules to improve logical and algorithmic thinking.
2. Relate concepts from Sanskrit texts to modern Engineering principles.
3. Develop simple computational models inspired by Sanskrit grammar/logics.
4. Use Sanskrit-based frameworks in AI, coding logic, or system design.
5. Identify interdisciplinary research opportunities combining Sanskrit & Engineering.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 1 | 2 | 1 | 1 |
| **CO2** | 2 | 1 | 2 | 2 | 1 |
| **CO3** | 3 | 1 | 2 | 3 | 1 |
| **CO4** | 2 | 2 | 2 | 2 | 1 |
| **CO5** | 3 | 2 | 2 | 2 | 1 |

**UNIT–I**

**Sanskrit as a Structured Language**

Sanskrit as rule-based system -Basics: alphabets, word formation (only essentials) -Sandhi as **data compression analogy** -Samasa as **modular design / block abstraction**-Simple sentence formation (very minimal grammar).

**UNIT–II**

**Sanskrit & Computational Thinking**

Paninian grammar → rule engine / compiler design -Shiva Sutras → encoding system-Binary concepts in Pingala (Chandas → digital logic) -Recursion & patterns in Sanskrit structures

**UNIT–III**

**Sanskrit in Core Engineering Domains**

**Civil / Mechanical:**

Sulba Sutras → geometry, measurements -Ancient construction logic → modular design

**Electrical / ECE:**
Concept of energy (Agni, Surya) → symbolic + physical mapping -Wave & sound (Nada → signal analogy)
**Systems Thinking:** Interconnectedness → system design philosophy

**UNIT–IV**
**Sanskrit & Modern Technology**
Sanskrit & Artificial Intelligence (knowledge representation) -Natural Language Processing (NLP) -Formal languages & syntax -Command-based structures → programming analogy

**UNIT–V**
**Mini Applications & Case Studies**
Case study: Sanskrit → Algorithm (simple flowchart) -Chandas → binary pattern generation-Design a simple rule-based system using Sanskrit logic -Mini presentation / activity

## TEXT BOOKS :


1. **Kapil Kapoor** – Language, Linguistics and Literature- Indian Perspective ; Academic Foundation, New Delhi; 1994 (1st Edition); **ISBN:** 978-8171880577
2. **Frits Staal** : *A Reader on the Sanskrit Grammarians;* MIT Press / Motilal Banarsidass ; 1972 (Original); **ISBN:** 978-0262191340
3. **George Gheverghese Joseph:** The Crest of the Peacock"; Princeton University Press; 2000 (2nd Edition; widely used); **ISBN:** 978-0691135267
4. B.V. Subbarayappa: "Indian Scientific Heritage" – National Institute of Advanced Studies (NIAS), Bangalore; 2006 **ISBN:** 978-8185015026
5. – M. Krishnamachariar : "History of Sanskrit Literature"; Motilal Banarsidass Publishers; Reprint 1993 (Original: 1937, TTD Press); **ISBN:** 978-8120802841


## SUGGESTED READING :


1. Pingala. *Chandah Shastra* (various editions, Nirnaya Sagar Press / Chowkhamba).
2. Bharati, A., et al. *Natural Language Processing: A Paninian Perspective*, PHI, 1995.
3. Selected IEEE / Springer Papers on Sanskrit & AI.

**26EGA103**

# STRESS MANAGEMENT BY YOGA

**(Audit Course)**

| | |
|---|---|
| Instruction | 2L Hours per Week |
| Duration of SEE | 2 Hours |
| SEE | 50 Marks |
| CIE | - |
| Credits | - |

**PREREQUISITE**: Knowledge on Yoga Practices.

**COURSE OBJECTIVES**:

**This course aims to:**

1. Create awareness about different types of stress and the role of yoga in the management of stress.
2. Promote positive health and overall well-being (Physical, mental, emotional, social and spiritual).
3. Prevent stress related health problems by yoga practice.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Understand yoga and its benefits.
2. Enhance Physical strength and flexibility.
3. Learn to relax and focus.
4. Relieve physical and mental tension through asanas
5. Improve work performance and efficiency

## CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 1 | 1 | - | - | 1 |
| **CO2** | 1 | 1 | - | - | 1 |
| **CO3** | 1 | 1 | - | - | 1 |
| **CO4** | 1 | 1 | - | - | 1 |
| **CO5** | 1 | 1 | - | - | 1 |

**UNIT - I**

**Meaning and definition of Yoga -** Historical perspective of Yoga - Principles of Astanga Yoga by Patanjali).

**UNIT - II**

**Meaning and definition of Stress** - Types of stress - Eustress and Distress. Anticipatory Anxiety and Intense Anxiety and depression. Meaning of Management- Stress Management.

**UNIT - III**

**Concept of Stress according to Yoga** - Stress assessment methods - Role of Asana, Pranayama and Meditation in the management of stress.

**UNIT - IV**

**Asanas**- (5 Asanas in each posture) - Warm up - Standing Asanas - Sitting Asanas - Prone Asanas - Supine asanas - Surya Namaskar

**UNIT – V**

**Pranayama-** Anulom and Vilom Pranayama - Nadishudhi Pranayama - Kapalabhati Pranayama - Bhramari Pranayama - Nadanusandhana Pranayama.

**Meditation techniques:** Om Meditation - Cyclic meditation: Instant Relaxation technique (QRT), Quick Relaxation Technique (QRT), Deep Relaxation Technique (DRT)

**TEXT BOOKS:**


1. Janardhan, Swami, "Yogic Asanas for Group Training - Part-I": Yogabhyasi Mandal, Nagpur.
2. Vivikananda, Swami**.** "Rajayoga or Conquering the Internal Nature", Advaita Ashrama (Publication Department), Kolkata.
3. Nagendra H.R and R. Nagaratna, "Yoga Perspective in Stress Management", Swami Vivekananda Yoga Prakashan, Bangalore.


**ONLINE RESOURCES:**

1. https://onlinecourses.nptel.ac.in/noc16_ge04/preview
2. https://freevideolectures.com/course/3539/indian-philosophy/11

**26ECA101**

# VALUE EDUCATION

**(Audit Course)**

| | |
|---|---|
| Instruction | 2L Hours per Week |
| Duration of SEE | 2 Hours |
| SEE | 50 Marks |
| CIE | - |
| Credits | - |

**COURSE OBJECTIVES:**

**This course aims to**

1. Understand Value Education, Self-development and National development.
2. Imbibe good human values and Morals in students.
3. Cultivate individual and National character.

**COURSE OUTCOMES:**

**After the completion of this course, the student will be able to**

1. Summarize classification of values and values for self-development.
2. Identify the importance of values in personal and professional life.
3. Apply the importance of social values for better career and relationships.
4. Analyze ethical issues in modern technology
5. Discuss concept of soul and reincarnation and promote responsible citizenship

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO1** | 2 | 2 | 2 | 2 | 3 |
| **CO2** | 2 | 2 | 2 | 2 | 3 |
| **CO3** | 2 | 2 | 2 | 2 | 3 |
| **CO4** | 2 | 2 | 2 | 2 | 3 |
| **CO5** | 2 | 2 | 2 | 2 | 3 |

**UNIT - I**

**Human Values, Ethics and Morals:** Concept of Values, Human Values, Indian concept of humanism, Values for self-development, Social values, Individual attitudes, Work ethics, Moral and non- moral behavior, Standards and Principles based on religion, Culture and Tradition.

**UNIT - II**

**Value Cultivation, and Self-Management:** Need and Importance of cultivation of values such as Sense-of Duty,
Devotion to work, Self-reliance, Confidence, Concentration, Integrity & discipline, and Truthfulness.

**UNIT - III**

**Spiritual Outlook and Social Values:** Personality and Behaviour Development, Scientific attitude and Spiritual (soul) outlook, Cultivation of Social Values Such as Positive Thinking, Punctuality, Love & Kindness, Avoiding fault finding in others, Reduction of anger, Forgiveness, Dignity of labour, True friendship, Universal brotherhood and religious tolerance., Happiness Vs Suffering, Love for truth, Aware of self-destructive habits, Appreciation and co-operation.

**UNIT - IV**

**Technology, Society, and Sustainability:** Ethics in emerging technologies (AI, Data, 5G, IoT); Privacy and cybersecurity, Environmental ethics and sustainable development; Social responsibility of engineers, Policy and governance.

**UNIT - V**

**Universal Values and Global Perspectives:** Mind your mind, Self-control**,** Concept of soul, Science of Reincarnation, Concepts of Dharma and Karma, The qualities of Devine and Devilish, Satwic, Rajasic and Tamasicgunas. Global citizenship, Happiness and meaningful life.

**TEXT BOOKS:**


1. Chakroborty, S.K. "Values & Ethics for organizations Theory and practice", Oxford University Press, New Delhi, 1998.
2. Jaya Dayal Goyandaka, "Srimad Bhagavad Gita", with Sanskrit Text, Word meaning and Prose meaning, Gita Press, Gorakhpur, 2017.


**REFERENCE BOOKS:**


1. George Reynolds, Ethics in Information Technology, 6th Edition, Cengage Learning, 2018
2. Melanie Mitchell, Artificial Intelligence: A Guide for Thinking Humans, 1st Edition, Farrar, Straus and Giroux, 2019.

**26CSO101**

## BUSINESS ANALYTICS
(Open Elective)

| | |
|---|---|
| Instruction | 3L Hours per Week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**PRE-REQUISITES:** Basic of programming, basic mathematics**.**

**COURSE OBJECTIVES:**

**This course aims to:**

1. Understanding the basic concepts of business analytics and applications.
2. Study various business analytics methods including predictive, prescriptive and descriptive analytics.
3. Prepare the students to model business data using various data mining, decision making methods.

**COURSE OUTCOMES:**

**After completion of this course, students will be able to:**

1. Identify and describe complex business problems in terms of analytical models.
2. Apply appropriate analytical methods to solve business problems and interpret the resulting metrics and measures to achieve stated objectives.
3. Illustrate descriptive, predictive and prescriptive analytics methods and techniques.
4. Model business data using data mining, forecasting, decision tree, and clustering techniques.
5. Design and evaluate viable data-driven solutions to complex business decision-making problems.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO 1** | 3 | 1 | 2 | 2 | 1 |
| **CO 2** | 3 | 2 | 3 | 2 | 2 |
| **CO 3** | 2 | 2 | 3 | 2 | 2 |
| **CO 4** | 3 | 2 | 3 | 2 | 2 |
| **CO 5** | 3 | 3 | 3 | 3 | 3 |

**UNIT - I**

**Introduction to Business Analytics:** Introduction to Business Analytics, need and science of data driven decision making, Descriptive, predictive, prescriptive analytics and techniques, Big data analytics, Web and Social media analytics, Machine Learning algorithms, Generative AI , LLMs and Explainable AI (XAI) in business analytics, framework for decision making, challenges in data driven decision making and future.

**UNIT - II**

**Descriptive Analytics:** Introduction, data types and scales, types of measurement scales, population and samples, measures of central tendency, percentile, decile and quadrille, measures of variation, measures of shape-skewness, data visualization.

**UNIT - III**

**Forecasting Techniques:** Introduction, time-series data and components, forecasting accuracy, moving average method, single exponential smoothing, Holt's method, Holt-Winter model, Croston's forecasting method, regression model for forecasting, Auto regression models, auto-regressive moving process, ARIMA, Theil's coefficient

**UNIT - IV**

**Decision Trees:** CHAID, Classification and Regression tree, splitting criteria, Ensemble methods, Random Forest, XGBoost. Clustering: Distance and similarity measures used in clustering, Clustering algorithms, K-Means, Prescriptive Analytics- Linear Programming (LP) and LP model building.

**UNIT-V**

**Six Sigma:** Introduction, origin, 3-Sigma Vs Six-Sigma process,cost of poor quality, industry applications, six sigma measures, DPMO, yield, sigma score, DMAIC methodology, Six Sigma toolbox.

**TEXTBOOKS:**


1. U Dinesh Kumar, "Business Analytics", Wiley Publications, 2nd Edition, 2022
2. Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, "Business analytics Principles,Concepts, and Applications with SAS", Associate Publishers, 2015


**SUGGESTED READINGS:**


1. S. Christian Albright, Wayne L. Winston, "Business Analytics - Data Analysis and Decision Making",6th Edition, Cengage, 2020.


**ONLINE RESOURCES:**

1. Coursera – Business Analytics Specialization (University of Pennsylvania, Wharton): https://www.coursera.org/specializations/business-analytics
2. NPTEL – Business Analytics and Data Mining (IIT Roorkee): https://nptel.ac.in/courses/110107106
3. edX – Data Science and Analytics MicroMasters (MIT): https://www.edx.org/micromasters/mitx-statistics-and-data-science.

**26MEO103**

## COMPOSITE MATERIALS

(Open Elective)

| | |
|---|---|
| Instruction | 3L Hours per Week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**COURSE OBJECTIVES**:

**This course aims to:**

1. Provide concepts of Composite materials and their constituents.
2. Explain the Classification of the reinforcements and matrix materials.
3. Provide Fabrication methods of metal matrix composites.
4. Explain manufacturing of Polymer matrix composites.
5. Elucidate Failure mechanisms in composite materials.

**COURSE OUTCOMES**:

**Upon completion of this course, students will be able to:**

1. Understand composite materials and their reinforcements.
2. Summarize micro-mechanics approach as applied to UD lamina.
3. Apply fabrication methods of metal, ceramic and carbon matrix composites.
4. Apply fabrication methods of polymer matrix composites..
5. Analyze the lamina and laminate from failure perspective.

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO 1** | 3 | 1 | 3 | 1 | - |
| **CO 2** | 3 | 1 | 3 | 1 | - |
| **CO 3** | 3 | 1 | 3 | 1 | - |
| **CO 4** | 3 | 1 | 3 | 1 | - |
| **CO 5** | 3 | 1 | 3 | 1 | - |

**UNIT - I**

**Introduction:** Definition Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

**UNIT - II**

**Reinforcements**: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements.

**Mechanical Behaviour of composites**: Rule of mixtures, Inverse rule of mixtures. Iso-strain and Iso-stress conditions.

**UNIT- III**

**Processing of Metal Matrix Composites:** Casting - Solid State diffusion technique, Cladding - Hot isostatic pressing. Properties and applications.

**Processing of Ceramic Matrix Composites:** Liquid Metal Infiltration - Liquid phase sintering.

**Processing of Carbon - Carbon composites:** Knitting, Braiding, Weaving. Properties and applications.

**UNIT - IV**

**Processing of Polymer Matrix Composites:** Preparation of Moulding compounds and prepregs - hand layup method - Autoclave method - Filament winding method - Compression moulding - Reaction injection moulding. Properties and applications.

**UNIT - V**

**Strength:** Lamina Failure Criteria, strength ratio, maximum stress criteria, maximum strain criteria, interactive failure criteria and hygrothermal failure. Laminate first ply failure -insight strength**.**

**TEXT BOOKS:**


1. K.K.Chawla, "Composite Materials- Science and Engineering", 4th edition, Springer Verlag, 2019.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007..
3. R.M. Jones. Mechanics of Composite Materials. 2 nd ed. CRC press. 2018.


**SUGGESTED READING:**


1. Deborah D.L. Chung, "Composite Materials Science and Applications" 2nd edition, Springer Verlag, 2010.
2. Sanjay K. Mazumdar, "Composites Manufacturing- materials, product and process engineering", 1st edition, CRC press, 2002.
3. Daniel Gay, "Composite Materials Design and Applications" 3rd edition, CRC press, 2015.

**26CEO101**

## COST MANAGEMENT OF ENGINEERING PROJECTS

(Open Elective)

| | |
|---|---|
| Instruction | 3L Hours per week |
| Duration | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**COURSE OBJECTIVES:**

**This course aims to:**

1. To enable the students to understand the concepts of Project management.
2. To provide knowledge on concepts of Project Planning and scheduling.
3. To create an awareness on Project Monitoring and Cost Analysis
4. To provide adequate knowledge to the students on Recourse Management Costing-Variance Analysis
5. To train the students with the concepts of Budgetary Control for cost management and to provide basic platform on Quantitative techniques for cost management.

**COURSE OUTCOMES:**

**After the completion of this course, the student will be able to**

1. Acquire in-depth knowledge about the concepts of project management and understand the principles of project management
2. Determine the critical path of a typical project using CPM and PERT techniques.
3. Prepare a work break down plan and perform linear scheduling using various methods.
4. Solve problems of resource scheduling and levelling using network diagrams.
5. Learn the concepts of budgetary control and apply quantitative techniques for optimizing project cost.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO 1** | 1 | 1 | -- | 1 | - |
| **CO 2** | 1 | 2 | 1 | 1 | - |
| **CO 3** | 1 | 1 | 1 | 1 | - |
| **CO 4** | 2 | 2 | 1 | 1 | - |
| **CO 5** | -- | 1 | 1 | 1 | - |

**UNIT- I**

**Project Management:** Introduction to project managements, stakeholders, roles, responsibilities and functional relationships. Principles of project management, objectives and project management system. Project team, organization, roles, and responsibilities. Concepts of project planning, monitoring, staffing, scheduling and controlling.

**UNIT- II**

**Project Planning and Scheduling:** Introduction for project planning, defining activities and their interdependency, time and resource estimation. Work break down structure. Linear scheduling methods-bar charts, Line of Balance (LOB), their limitations. Principles, definitions of network-based scheduling methods: CPM, PERT. Network representation, network analysis-forward and backward passes.

**UNIT- III**

**Project Monitoring and Cost Analysis:** introduction-Cost concepts in decision making; relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision- Making, Time cost trade off Crashing project schedules, its impact on time on time, cost. Project direct and indirect costs.

**UNIT- IV**

**Resources Management and Costing-Variance Analysis:** Planning, Enterprise Resource Planning, Resource scheduling and levelling. Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis

**Standard Costing and Variance Analysis.** Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement.

**UNIT- V**

**Boundary Budgetary Control: Flexible Budgets;** Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

**Quantitative techniques for cost management:** Linear Programming, PERT/CPM, Transportation Assignment problems, Simulation, Learning Curve Theory.

**TEXT BOOKS:**


1. Charles T Horngren "Cost Accounting A Managerial Emphasis", Pearson Education; 14 edition (2012),
2. Charles T. Horngren and George Foster, "Advanced Management Accounting" Prentice-Hall; 6th Revised edition (1 February1987)
3. Robert S Kaplan Anthony A. Atkinson, "Management & Cost Accounting", Pearson; 2 edition (18 October1996)


**SUGGESTED READING:**


1. *K. K Chitkara, "Construction Project Management: Planning, scheduling and controlling", Tata McGrawHill Education. (2004).*
2. *Kumar Neeraj Jha "Construction Project Management Theory and Practice", Pearson Education India; 2 edition (2015).*

**26MEO101**

# INDUSTRIAL SAFETY

(Open Elective)

| | |
|---|---|
| Instruction | 3L Hours per Week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**COURSE OBJECTIVES**:

**This course aims to cover:**

1. Causes for industrial accidents, preventive steps to be taken, Factories act 1948 and 5S Techniques.
2. Fundamental concepts of Maintenance Engineering.
3. About Safety in advanced manufacturing systems.
4. The basic concepts and importance of fault tracing.
5. The steps involved in periodic and preventive maintenance of various industrial equipments.

**COURSE OUTCOMES**:

**Upon completion of this course, students will be able to:**

1. Identify causes of industrial accidents and recommend preventive measures.
2. Select appropriate tools and practices for various maintenance procedures.
3. Apply different Safety measures in advanced manufacturing systems.
4. Diagnose faults in equipment such as machine tools, IC engines, and boilers.
5. Implement periodic and preventive maintenance for industrial equipment including motors, pumps, air compressors, and machine tools.

## CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO 1** | 3 | 3 | 2 | 2 | 1 |
| **CO 2** | 3 | 3 | 2 | 2 | 1 |
| **CO 3** | 3 | 3 | 2 | 2 | 1 |
| **CO 4** | 3 | 3 | 2 | 2 | 1 |
| **CO 5** | 3 | 3 | 3 | 2 | 1 |

## UNIT - I

## SAFETY MANAGEMENT CONCEPTS AND INDUSTRIAL SAFETY PRACTICES

**Industrial Safety & Legal Aspects:** Industrial accidents – causes, types, consequences, and preventive measures. Mechanical and electrical hazards and their control. Fire hazards, prevention and firefighting methods. Safety color codes and safety signage. Salient provisions of the Factories Act 1948 related to health, safety, and welfare.

**Safety Audit:** Types of safety audits – audit methodology, preparation of audit checklists, Non-Conformity Reporting (NCR). Analysis and interpretation of accident records and safety reports.

**5S Techniques:** Introduction, objectives, and elements of 5S (Sort, Set in order, Shine, Standardize, Sustain). Benefits of 5S in enhancing workplace safety, productivity, and efficiency.

## UNIT - II

**Fundamentals of Maintenance Engineering:** Definition and objectives of maintenance engineering. Primary and secondary functions and responsibilities of the maintenance department. Types of maintenance (preventive, predictive, breakdown, corrective) and their applications. Tools and equipment used in maintenance activities. Maintenance cost and its relationship with replacement

decisions and economy. Concept of service life and factors affecting the lifespan of equipment.

**UNIT- III**

**Safety in advanced manufacturing systems:** Machine safety in CNC, robotics, and Flexible Manufacturing Systems (FMS). Human–machine interaction safety. Safety in Industry 4.0 environments including cyber-physical systems, smart factories, and digital twins. Safety in additive manufacturing (powder handling and laser safety). Safety in material handling systems (conveyors, cranes, AGVs) and manufacturing processes (welding, casting, forging, machining). Electrical safety in automation and Lockout/Tagout (LOTO) procedures.

**UNIT - IV**

**Fault Tracing:** Concept and importance of fault tracing. Decision tree approach – need, structure, and applications. Sequence of fault-finding activities and systematic troubleshooting procedures. Development and representation of fault diagnosis using decision trees. Fault tracing in industrial equipment including machine tools, pumps, air compressors, internal combustion engines, boilers, and electrical motors. Types of faults in machine tools and their general causes.

**UNIT - V**

**Maintenance and Condition Monitoring**

**Periodic and Preventive Maintenance:** Periodic inspection, concept and need. Cleaning, servicing, and overhauling of mechanical components and electrical motors. Common motor faults and remedies. Preventive maintenance definition, steps, and advantages. Maintenance procedures for machine tools, pumps, air compressors, and DG sets.

**Condition monitoring and basic concepts of Proactive maintenance for Industry 4.0.**

**TEXT BOOKS:**


1. L. M. Deshmukh, Industrial Safety Management, McGraw Hill Education, New Delhi, 1st Edition, 2010.
2. M.R. Sahoo, Industrial Safety Engineering, RK Publications, New Delhi, 1st Edition, 2015.
3. H. P. Garg, “Industrial Maintenance”, S. Chand and Company, may 1987.
4. Das Akhil Kumar, Principles of Industrial Safety Management Understanding the Ws of Safety at Work, Second edition, PHI Learning Pvt Ltd, Jan 2020


**SUGGESTED READING:**


1. Parth B. Shah, Industrial Safety and Maintenance Engineering, Technical publications, 2021.
2. Higgins & Morrow, “Maintenance Engineering Handbook”, McGraw-Hill Education Eighth Edition, February 2014.
3. M.P. Poonia, S.C. Sharma, Khanna Publishing House - Technology & Engineering, year 2019.

**26MEO102**

## INTRODUCTION TO OPTIMIZATION TECHNIQUES

(Open Elective)

| | |
|---|---|
| Instruction | 3 L Hours per Week |
| Duration of SEE | 3 Hours |
| SEE | 60 Marks |
| CIE | 40 Marks |
| Credits | 3 |

**COURSE OBJECTIVES**:

**This course aims to:**

1. Understand the LPP models.
2. Understand the Transportation and Assignment techniques.
3. Understand the procedure of Project Management along with CPM and PERT techniques.
4. Understand the concepts of queuing theory and inventory models.
5. Understand sequencing techniques.

**COURSE OUTCOMES**:

**Upon completion of this course, students will be able to:**

1. Formulate a linear programming problems (LPP).
2. Build and solve Transportation Models and Assignment Models.
3. Apply project management techniques like CPM and PERT to plan and execute project successfully.
4. Apply queuing and inventory concepts in industrial applications.
5. Apply sequencing models in industries.

### CO-PO ARTICULATION MATRIX

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO 1** | 3 | 1 | 3 | 1 | 2 |
| **CO 2** | 3 | 1 | 3 | 1 | 2 |
| **CO 3** | 1 | 1 | 3 | 2 | 3 |
| **CO 4** | 2 | 1 | 3 | 2 | 2 |
| **CO 5** | 2 | 1 | 3 | 2 | 2 |

**UNIT - I**

**Operations Research**: Definition, Scope, Models, Linear programming problems (LPP), Formulation, Graphical Method, and Simplex Method.

**UNIT - II**

**Transportation Models**: Finding an initial feasible solution, North West corner method, Least cost method, Vogel's approximation method, Finding the optimal solution, Special cases in transportation problems, Unbalanced transportation problem, Degeneracy in transportation, Profit maximization in transportation.

**UNIT- III**

**Project Management**: Definition, Procedure and objectives of project management, Differences between PERT and CPM, Rules for drawing network diagram, Scheduling the activities, Fulkerson's rule, Earliest and latest times, Determination of ES and EF times in forward path, LS & LF times in backward path, Determination of critical path, Duration of the project, Free float, Independent float and total float.

**UNIT - IV**

**Queuing Theory and Inventory:** Kendols notation, Single server models, Inventory control, Deterministic inventory models, Probabilistic inventory control models.

**UNIT - V**

**Sequencing Models**: Introduction, Objectives, General assumptions, Processing 'n' jobs through two machines, Processing 'n' jobs through three machines**.**

**TEXT BOOKS:**


1. H.A. Taha, Operations Research, An Introduction, PHI, 2008.
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008.


**SUGGESTED READING:**


1. Hitler Libermann, Operations Research, McGraw Hill Pub, 2009.
2. Harvey M Wagner, Principles of Operations Research, Prentice Hall of India, 2010.

**26EEO102**

## ELECTRIC VEHICLES & FUTURE MOBILITY

(Open Elective)

| | |
|---|---|
| Instruction: | 3L Hours per Week |
| Duration of SEE: | 3 Hours |
| SEE: | 60 Marks |
| CIE: | 40 Marks |
| Credits: | 3 |

**PREREQUISITE:**No prior knowledge required. Basic understanding of science is sufficient.

**COURSE OBJECTIVES:**

**This course aims to:**

1. Introduce the fundamentals of electric vehicles and their importance in modern transportation.
2. Explain the basic components and working of electric vehicles.
3. Familiarize students with battery technologies and charging infrastructure.
4. Create awareness about environmental benefits and challenges of EV adoption.
5. Provide insights into future mobility trends including smart transportation systems.

**COURSE OUTCOMES:**

**Upon completion of this course, students will be able to:**

1. Understand the basic concepts and need for electric vehicles.
2. Explain the components and working principles of EV systems.
3. Analyze battery technologies and charging methods.
4. Evaluate the environmental and economic impact of EVs.
5. Appreciate future mobility trends and emerging transportation technologies.

**CO-PO ARTICULATION MATRIX**

| CO/PO | PO1 | PO2 | PO3 | PO4 | PO5 |
|---|---|---|---|---|---|
| **CO 1** | 1 | 1 | 1 | 1 | 1 |
| **CO 2** | 2 | 1 | 1 | 1 | 1 |
| **CO 3** | 2 | 2 | 1 | 2 | 1 |
| **CO 4** | 1 | - | - | 2 | 1 |
| **CO 5** | 2 | 2 | 1 | 1 | 1 |

**UNIT – I**

**Introduction to Electric Vehicles:** History and evolution of transportation.-Need for electric mobility – energy crisis and environmental concerns.-Types of vehicles: Conventional, Hybrid, Plug-in Hybrid, Battery Electric Vehicles (BEV).-Basic comparison between IC engine vehicles and electric vehicles. Overview of EV ecosystem.

**UNIT – II**

**Components and Working of Electric Vehicles:** Main components: Electric motor -Battery pack -Controller and power electronics -Transmission system -Working principle of EVs.-Types of motors used in EVs (overview).-Regenerative braking concept.

**UNIT – III**

**Batteries and Charging Infrastructure:** Battery basics – types (Lead-acid, Lithium-ion, emerging technologies).-Battery parameters – capacity, energy density, charging cycles.-Charging methods: Slow charging; Fast charging; Wireless charging (intro) -Charging infrastructure – public and private charging stations.

Battery management system (BMS) – basic concept**.**

**UNIT – IV**

**Environmental and Economic Aspects:** Environmental impact of EVs – emissions comparison.-Lifecycle analysis (production to disposal).-Cost comparison – EV vs conventional vehicles.-Government policies and incentives (India focus).-Challenges in EV adoption – range anxiety, infrastructure, cost.

**UNIT – V**

**Future Mobility and Emerging Trends:** Smart mobility and intelligent transportation systems.-Electric public transport – buses, metros. Autonomous and connected vehicles (intro).-Vehicle-to-Grid (V2G) concept.-Future trends: Sustainable mobility, shared mobility, green transportation.

**TEXTBOOKS:**

1. James Larminie & John Lowry, *Electric Vehicle Technology Explained*, Wiley.
2. Mehrdad Ehsani et al., *Modern Electric, Hybrid Electric and Fuel Cell Vehicles*, CRC Press.
3. Government of India, *EV Policy Reports and Mobility Guidelines*.

**SUGGESTED READING:**

1. NITI Aayog, *India Electric Mobility Reports*.
2. International Energy Agency (IEA), *Global EV Outlook*.
3. Bureau of Energy Efficiency (BEE), EV awareness materials.
4. IEEE Journals on Electric Mobility.

**NPTEL / Online Resources:**

| S.No | Course Name | Instructor | Institute |
|---|---|---|---|
| 1 | Electric Vehicles | Prof. S. Banerjee | IIT Kharagpur |
| **Other Online Resources:** | | | |
| 1 | https://nptel.ac.in | | |
| 2 | https://niti.gov.in | | |
| 3 | https://iea.org | | |