DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Minutes of the Meeting of Programme Assessment and Quality Improvement Committee (PAQIC) ME (ES&VLSID) Program AY 2025-26

Date: 25 April 2026 **Time:** 10.30 AM **Mode:** Online

Agenda of the Meeting

1. Approval of Previous year minutes
2. Review of Academic Performance
3. Advanced Course Delivery & Pedagogy
4. CO–PO–PSO Attainment Analysis
5. Research & Thesis Progress
6. Laboratory & Research Infrastructure
7. Internships & Industry Interaction
8. Curriculum Enrichment
9. Student Research & Innovation
10. Placement & Higher Studies
11. Accreditation & Quality Compliance (NBA/NAAC)
12. New Initiatives
13. Any other point with the permission of the chair.

Members Present

S. No.	Name and Designation	Designation
1.	Dr. K.Vasanth, HoD, ECE Dept., CBIT	Chairperson
2.	Dr. B.Khaleelu Rehman. Associate.Professor, ECE Dept., CBIT	Convener
,3.	Sri. Linga Viswanath Sr.SOC Manager,Central R&D, Si Labs, Hyderabad	Member
4.	Sri. Anasuri Raghuveer Asst. Engineer, Doordarshan, Hyderabad.	Member
5.	Sri. T.Uday Kiran MTS Silicon Design Engineer, AMD India Pvt Ltd, Hyderabad	Member
6	Sri. P. Bhanu Srinivas Scientist – F, RCI, Hyderabad	Member
7.	Dr M Sushanth Babu Professor, Chairman- Miscellaneous – CEG, Dept. of ECE, CBIT	Member
8.	Dr M.Ramana Reddy Assistant Professor, PG NBA Coordinator, Dept. of ECE, CBIT	Member
9.	In-charges of CEG pertaining to this Program	Member

Minutes of the Meeting

The HoD has welcomed all the external and internal members and he enumerated the above agenda points in comparison with AY 2023-24, 2024-25, 2025-26

1. Approval of Minuites of PAQIC meeting 2025

The Committee approved the previous PAQIC meeting

2. Department Profile & Academic Activities

- Overview of department vision, mission, and organizational structure presented.
- ME Embedded Systems & VLSI Design program reaccredited (latest cycle: 2024).
- Department faculty strength: 44 teaching staff.
- PhD-qualified faculty: ~83.3%.
- Strong gender diversity maintained among faculty members.

3. Teaching–Learning Process

- Courses are allocated based on academic calendar and lesson planning.
- Continuous Internal Evaluation (CIE) includes:
  - Assignments
  - Slip tests
  - Internal exams
  - Course projects
- Course delivery monitored through: Course Audit I, II and III
- Innovative teaching methodologies adopted:
  - Mind mapping
  - Think–pair–share
  - Classroom discussions
  - Online learning resources
  - Mentimeter-based interaction tools
- Direct feedback taken from students on Faculty: Overall improvement of.18% in scores above 75% over last three years.

4. Faculty Development Activities

- 94 NPTEL/SWAYAM certifications completed.
- Several faculties ranked in Top 1%, 2%, and 5%.
- Over 130 academic events organized:
  - FDPs
  - Workshops
  - Guest lectures
  - Conferences
- 325 faculty participations recorded in training programs.
- 65% participation in premier institutes (IITs/NITs).

5. Student Performance & Outcomes

- Graduation success rate improved by ~6.7%.
- Majority of students secured distinction.
- Overall academic performance crossed 85.9%.
- Program Outcomes (POs) successfully attained for 2024 batch.

6. Curriculum Enhancement (R23 → R26)

Major improvements include:

- Shift from content-based learning to applied learning
- Strong alignment with NEP 2020
- Introduction of AI foundational courses
- Increased elective flexibility
- Early industry exposure
- Integration of experiential learning
- Transition toward global employability orientation

7. Industry–Institute Interaction

Department Industry Interaction Cell activities include:

- 12 active MoUs
- Industry co-teaching initiatives
- Industry-based evaluations
- 6 industrial visits conducted
- 100% industry exposure to students

Industry experts delivered lectures on:

- DSP architectures
- FPGA systems
- Embedded processor architectures

8. Internship, Placement & Higher Studies

- Internship participation increased by 133%
- Placement rate: **52%**
- Higher studies (MS/PhD): **33%**
- Entrepreneurship initiatives initiated by students

9. Research & Development Activities

Key achievements:

- 323 total publications in last 3 years
- 76 Scopus-indexed Q1 journal papers
- 223 indexed conference papers
- 9 granted patents in last 3 academic years
- 400% growth in patent filings

Sponsored research funding:

- ₹3.45 Crores ongoing projects
- ₹62.76 Lakhs sanctioned during current academic year

Seed-money project outcomes:

- Satellite ground station development
- Soldier monitoring system
- Borewell rescue system
- Smart building energy solutions
- Pandemic hygiene automation system

10. Laboratories & Centers of Excellence

Established facilities include:

- VLSI Lab (supported by MeitY)
- Navigation & Communication Research Centre
- Automatic Weather Monitoring Station
- Embedded Systems CoE with Pi Square Technologies
- Positioning, Navigation & Timing Lab (IIT Hyderabad collaboration)

11. Alumni Engagement

- Alumni network spread across:
  - 73 countries
  - 20 Indian states
- Alumni from organizations including:
  - Qualcomm
  - Amazon
  - DRDO
- Alumni talk conducted for career mentoring

- Sri. Linga Viswanath emphasized the importance of **strengthening foundations Artificial Intelligence (AI) integration** in the curriculum to enhance industry readiness of students.
    - The inclusion of AI-based laboratory components in the revised curriculum was appreciated.
    - Further he added that students must develop competencies beyond traditional coding environments using AI-enabled tools, as several routine coding tasks are gradually becoming obsolete due to the increasing adoption of AI-assisted development practices in the industry.
    - He also emphasized that industries are predominantly investing in AI tools to improve development quality and speed up engineering activities.
    - To this, the Head of the Department (HoD) responded that under the R26 curriculum, a Workshop Laboratory is being introduced for postgraduate students. This laboratory does not require any specific prerequisites and is designed to enable students to develop VLSI-based code, perform debugging, and implement system-level design tasks. The HoD further highlighted that such higher-order laboratory components are being established to enhance practical competency and industry readiness among students.
    - Sri. Linga Viswanath appreciated the efforts.
    - The Committee approved the scheme(I to IV semester) and syllabus (I and II semester) for (ME ES&VLSID) and permitted to get submit to BOS for further proceedings
- **Sri. P. Bhanu Srinivas recommended incorporating ethical aspects or morality of Artificial Intelligence** into the curriculum to ensure responsible usage of AI technologies and to create awareness among students about the societal implications of AI applications.
    - He suggested introducing **RISC-V architecture and reconfigurable system design concepts** in the curriculum to align the program with emerging trends in embedded systems and processor architecture.
- **Professor P. N. Sastry** appreciated the department's enhanced industry collaboration initiatives and suggested further strengthening the curriculum through increased industry-oriented components.
- **Dr. M.L.N. Acharyulu** suggested integrating AI-based tools into laboratory sessions to improve students' practical exposure and industry readiness.
- **Sri. T. Uday Kiran** appreciated the improvements made in the curriculum compared to the previous academic year, particularly the increased emphasis on the inclusion of Artificial Intelligence (AI) components.
    - The member further suggested that it is equally important to ensure that students are trained to verify and validate the correctness of AI-generated outputs.
    - It was emphasized that although AI tools can automatically generate code when specifications are clearly defined, students should develop the ability to critically evaluate and confirm the accuracy and reliability of such generated solutions.
- The Head of the Department informed the committee that the department has established strong infrastructure and laboratory support for **VLSI design**, and that students are being trained extensively in both **digital and analog VLSI** using industry-standard tools such as **Cadence, Synopsys, and other relevant platforms**. It was further mentioned that the department is among the pioneering institutions offering such advanced training and is on par with leading institutes such as Indian Institute of Technology Hyderabad in terms of available facilities and learning resources.
- The Head of the Department requested the industry representative to share possible inputs or leads through their organization's HR channels regarding internship and placement opportunities for students trained in VLSI tools. The industry representative responded

positively and assured that they would explore the possibility from their side and get back to the department with further information.

- The Committee members also hinted to have target to faculty, students and department for better performance in each academic Year.
- HoD presented a 1 Year & 5 Year Plan along with plan of actions planned for upcoming academic Years.

All the members including external members appreciated the comprehensive presentation given by the HoD.

Dr. K. Vasanth
PAQIC Chairperson

Copy to:
1. Principal for information
2. PAQIC Members
3. ECE Faculty ECE Dept.

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