

# DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## 3<sup>rd</sup> Board of Studies (BoS) – BE-EE(VLSI Design & Technology)

Date: 29-04-2026

Time: 3.00 PM

Mode: Hybrid (Online and Offline)

### Members Present:

S.No.	Member	Name	Designation
1.	Head of the Department	Dr. K. Vasanth, Associate Professor & Head of the Department	Chairperson
2.	External Member	Prof. S. Anuradha Professor Department of ECE, NIT Warangal.	Member
3.	External Member	Prof. P. Chandra Sekhar Principal, OUCE & Professor, Department of ECE	Member
4.	External Member	Deepak Raya PhD Scholar (PMRF) Neuroscience, IISc Bangalore	Member
5.	External Member	Dr. M.A. Mushahid Majeed CAD Software Developer and Application Manager, NXP semiconductors Ltd. Hyderabad	Member
6.	External Member	Ms. Kilaru Susrutha Reddy Silicon Design Engineer AMD, Hyderabad	Member
7.	Professor	Dr. N.V. Koteswara Rao Professor, Department of ECE, CBIT	Member
8.	Professor	Dr. D. Krishna Reddy Professor, Department of ECE, CBIT	Member
9.	Professor	Dr. P. Narahari Sastry Professor, Department of ECE, CBIT	Member
10.	Professor	Prof. Vivek Singh Kushwah, Professor, Department of ECE, CBIT	Member
11.	Associate Professor	Dr. B. Khaleelu Rehman Professor, Department of ECE, CBIT	Member

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12.	Assistant Professor	Dr. Mohd Ziauddin Jahangir Assistant Professor, Department of ECE, CBIT	Member
13.	Invited Member	Smt. Ghata Chauhan Assistant Professor, Department of ECE, CBIT	Invited Member

**Leave of Absence:** Ms. R. Hari Chandana, Sr. Engineer  
Dr. A.D. Sarma, Professor, Department of ECE, CBIT

### Minutes of the Meeting

The meeting began with a welcome address delivered on behalf of the Department of ECE, where all Board of Studies members and external experts were formally welcomed for the third BoS meeting focused on the R26 curriculum revision for EVL (VLSI Design and Technology). The purpose of the meeting was clearly stated as the review, discussion, and approval of the proposed R-26 curriculum framework.

HoD presented the R26 scheme, syllabus and process for regulation change. It was explained that the curriculum was developed based on feedback collected from various stakeholders such as students, alumni, academicians, industry experts, employers, and parents, and had already been reviewed in earlier committee meetings before being presented for final approval.

The R-26 curriculum was presented as an improved framework over R22A, focusing on AI integration, industry engagement, flexibility in learning, and alignment with NEP 2020. It emphasizes a shift from content-based learning to competency-based and application-oriented learning, multidisciplinary learning, and outcome-based assessment.

The discussion highlighted enhanced features such as early introduction of core subjects, inclusion of emerging technologies like AI, ML, IoT, and Quantum Computing, and increased opportunities for internships, industry certifications, and NPTEL-based learning.

It was also noted that the curriculum promotes global employability, innovation, and entrepreneurship while incorporating value-based and interdisciplinary courses in line with national education policies.

#### **Agenda 1: Approval of the minutes of the 2nd BoS Meeting held on 24-04-2025**

The minutes of the previous BoS meeting were reviewed and it was confirmed that all suggested modifications had been incorporated.

The committee approved the minutes without any further changes.

#### **Agenda 2: R22A – Curriculum / Syllabus Amendments for V & VI Sem (BE- EVL)**

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- It was proposed to include **8051 microcontroller content** in the Embedded System Design course (22EVC13), and accordingly two units covering 8051 were added.
- The incorporation of **8051-based experiments in the Embedded System Design Lab** was also presented.
- A proposal to introduce a **VLSI Fabrication Lab** in the curriculum and establish the same in the department was discussed.
- It was proposed to enhance the **System on Chip (22EVC14) course with more ASIC-related content** to align with industry requirements.
- Further, the inclusion of **ASIC-based experiments using CADENCE Digital tools in the SoC Lab** was discussed as it improves industry readiness and practical skills.

The members approved all the points as discussed without any modifications.

### **Agenda 3: Value Added Courses for BE (EVL) for Ay 2026-27**

The proposal to offer value-added courses including **Real-Time Operating System using QNX, Digital VLSI Tool, and Tools for Analog Design** was presented.

The committee recognized their relevance to industry needs and approved all the proposed courses.

### **Agenda 4: R-26 – Approval of Scheme (I to VIII Semester)**

The complete scheme of the R-26 curriculum for B.E. Electronics Engineering (VLSI Design and Technology) from first to eighth semester was presented. Courses like **“Artificial Intelligence Foundation and Application”** and **“Python Programming and Hardware Integration Lab”** are added in the I Sem and II Sem respectively of the proposed R-26 curriculum. The curriculum highlights included AI integration, industry exposure, flexible electives, and alignment with NEP 2020.

After discussion, the scheme was approved by the Board.

### **Agenda 5: Inclusion of NPTEL Courses for Additional Minor Engineering**

The BoS Chairman sought approval to include appropriate NPTEL courses for awarding an Additional Minor Engineering degree.

The committee granted approval, authorizing the Chairman to finalize the courses with internal review and circulate them to members.

### **Agenda 6: Any Other Items with Permission of the Chair**

No major additional items were raised. The members expressed satisfaction with the overall curriculum structure and its alignment with industry and academic requirements.

The meeting concluded with a vote of thanks by the Head of the Department.