4	Dr.S.Radha	Theorems	Network Analysis	Never Miss a Class

Name of The Subject: Digital system design using Verilog

Name of the Innovative teaching methodology employed: Never Miss a Class

Name of the Topic: State Machines and Allied topics

Name of the Faculty: Dr.S.Radha

E-Content: Prepared 7 videos on NA & S subject (ECE) and uploaded in Youtube

Sl. no.	Title of the E-Content module	Hosted on (web link)
1	FSM (mealey/ moore state diagram) to ASM Charts conversion	https://youtu.be/T_t1tYM5YN4
2	Delays in xor gate operation- verilog coding	https://youtu.be/355sDNPMIfA
3	cntrl signal(one) in buffer gate operation- verilog coding	https://youtu.be/ap-bK3X17Bw
4	cntrl signal(zero/one) in buffer gate operation- verilog coding	https://youtu.be/-mBInx3t8ao
5	cntrl signal(zero/one) in NOT gate operation- verilog coding	https://youtu.be/JnazeNAk4Xk
6	GSM in proteus using Arduino	https://youtu.be/Z4KOec1Tipg
7	GPS in proteus using Arduino	https://youtu.be/Ng7hnsTfgO0