PG-R23 Curriculum
With effective from 2023-24

ECE - Embedded Systems & VLSI Design

Scheme of Instruction and Syllabi of
M.E I to IV Semester of
Two Year Degree Course

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY
(An Autonomous Institute | Affiliated to Osmania University)
Accreditated by NBA & NAAC (A++)
Kokapet Village, Gandipet Mandal, Hyderabad -500075, Telanagana.
E-mail: principal@cbit.ac.in, Website: www.cbit.ac.in
Phone No. : 040-24193276 / 277 / 279

SCHEME OF INSTRUCTION AND SYLLABI

OF

MASTER OF ENGINEERING

FOR

EMBEDDED SYSTEMS & VLSI DESIGN

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)
Kokapet Village, Gandipet Mandal, Hyderabad– 500 075. Telangana
Accredited with NAAC- (A++)

E-Mail: principal@cbit.ac.in; Website: www.cbit.ac.in; Phone Nos.: 040-24193276 / 277 / 279

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)

VISION and MISSION of the INSTITUTE

VISION
To be a centre of excellence in technical education and research.

MISSION
To address the emerging needs through quality technical education and advanced research.

DEPARTMENT VISION & MISSION

VISION
To emerge as a vibrant model of excellence in education, research and innovation in Electronics and Communication Engineering.

MISSION

1. To impart strong theoretical and practical knowledge of the state of art technologies to meet growing challenges in the industry.
2. To carry out the advanced and need based research in consultation with the renowned research and industrial organizations.
3. To create entrepreneurship environment including innovation, incubation and encourage to patent the work.

PROGRAM EDUCATIONAL OBJECTIVES (PEOS)

1. Graduates will apply engineering expertise to solve real world problems in the areas of Embedded Systems and VLSI Design.
2. Graduates will have the ability to adopt latest technologies.
3. Graduates will be able to carry out research in the fields of Micro Electronics and Embedded Systems.
4. Graduates will develop professional ethics, effective communication skills, self-confidence and societal responsibilities.

PROGRAM SPECIFIC OUTCOMES (PSOS)

1. An ability to independently carry out research /investigation and development work to solve practical problems.
2. An ability to write and present a substantial technical report/document.
3. Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
4. Students will be able to use modern engineering tools/software to design and develop Embedded and VLSI Systems as per the needs of the Industry.
5. Students will be able to develop self-confidence, team work, skills for lifelong learning and committed to social responsibilities.

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)

Inline with AICTE Model Curriculum with effect from AY 2023-24

ME (EMBEDDED SYSTEMS & VLSI DESIGN)

SEMESTER – I

S.No	Course Code	Title of the Course	Scheme of Instruction			Scheme of Examination			Credits
			Hours per week			Duration of SEE in Hours	Maximum Marks		
			L	T	P/D		CIE	SEE	
THEORY									
1	23ECC201	Analog and Digital CMOS VLSI Design	3	--	--	3	40	60	3
2	23ECC202	Microcontrollers and Programmable Digital Signal Processors	3	--	--	3	40	60	3
3		Program Elective-I	3	--	--	3	40	60	3
4		Program Elective-II	3	--	--	3	40	60	3
5	23MEM103	Research Methodology and IPR	2	--	--	3	40	60	2
6		Audit Course-I	2	--	--	2	--	50	Non-Credit
PRACTICALS									
7	23ECC203	Analog and Digital CMOS VLSI Design Lab	--	--	3	--	50	--	1.5
8	23ECC204	Microcontrollers and programmable Digital Signal Processors Lab	--	--	3	--	50	--	1.5
Total			**16**	**--**	**6**	**17**	**300**	**350**	**17**
Clock Hours Per Week: 22									

L: Lecture	**D: Drawing**	**CIE: Continuous Internal Evaluation**
T: Tutorial	**P: Practical/Mini Project /Dissertation**	**SEE: Semester End Examination**

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)

Inline with AICTE Model Curriculum with effect from AY 2023-24

ME (EMBEDDED SYSTEMS & VLSI DESIGN)

SEMESTER – II

S.No	Course Code	Title of the Course	Scheme of Instruction			Scheme of Examination			Credits
			Hours per week			Duration of SEE in Hours	Maximum Marks		
			L	T	P/D		CIE	SEE	
THEORY									
1	23ECC205	IoT and RTOS based Embedded System Design	3	--	--	3	40	60	3
2	23ECC206	VLSI Design, Verification and Testing	3	--	--	3	40	60	3
3	23ECC207	Mixed Signal and RF IC Design	3	--	--	3	40	60	3
4		Program Elective-III	3	--	--	3	40	60	3
5		Program Elective-IV	3	--	--	3	40	60	3
PRACTICALS									
6	23ECC208	IoT and RTOS based Embedded System Design Lab	--	--	3	--	50	--	1.5
7	23ECC209	RTL Synthesis, Simulation and Verification Lab	--	--	3	--	50	--	1.5
8	23ECC210	Mini Project	--	--	2	--	50	--	1
Total			**15**	**--**	**8**	**15**	**350**	**300**	**19**
Clock Hours Per Week: 23									

L: Lecture	**D: Drawing**	**CIE: Continuous Internal Evaluation**
T: Tutorial	**P: Practical/Mini Project/ Dissertation**	**SEE: Semester End Examination**

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)

Inline with AICTE Model Curriculum with effect from AY 2023-24

ME (EMBEDDED SYSTEMS & VLSI DESIGN)

SEMESTER – III

S.No	Course Code	Title of the Course	Scheme of Instruction			Scheme of Examination			Credits
			Hours per week			Duration of SEE in Hours	Maximum Marks		
			L	T	P/D		CIE	SEE	
THEORY									
1		Program Elective-V	3	--	--	3	40	60	3
2		Open Elective	3	--	--	3	40	60	3
3		Audit Course-II	2	--	--	2	--	50	Non-Credit
DISSERTATION									
4	23ECC211	Industrial Project / Dissertation Phase I	--	--	20	--	100	--	10
Total			**8**	**--**	**20**	**8**	**180**	**170**	**16**
Clock Hours Per Week: 28									

L: Lecture	**D: Drawing**	**CIE: Continuous Internal Evaluation**
T: Tutorial	**P: Practical/Mini Project / Dissertation**	**SEE: Semester End Examination**

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)

Inline with AICTE Model Curriculum with effect from AY 2023-24

ME (EMBEDDED SYSTEMS & VLSI DESIGN)

SEMESTER – IV

S.No	Course Code	Title of the Course	Scheme of Instruction			Scheme of Examination			Credits
			Hours per week			Duration of SEE in Hours	Maximum Marks		
			L	T	P/D		CIE	SEE	
DISSERTATION									
1	23ECC212	Industrial Project / Dissertation Phase II	--	--	32	Viva-Voce	100	100	16
Total			**--**	**--**	**32**	**--**	**100**	**100**	**16**
Clock Hours Per Week: 32									

L: Lecture	**D: Drawing**	**CIE: Continuous Internal Evaluation**
T: Tutorial	**P: Practical/Mini Project /Dissertation**	**SEE: Semester End Examination**

LIST OF SUBJECTS FOR ME (ES & VLSI DESIGN) COURSE WITH SPECIALIZATION IN

S.No	Course Code	Title of the Course
PROGRAM CORE COURSES		
1.	23ECC201	Analog and Digital CMOS VLSI Design
2.	23ECC202	Microcontrollers and Programmable Digital Signal Processors
3.	23ECC205	IoT and RTOS based Embedded System Design
4.	23ECC206	VLSI Design, Verification and Testing
5.	23ECC207	Mixed Signal and RF IC Design
PRACTICAL COURSES / MINI PROJECT WITH SEMINAR/ DISSERTATION		
6.	23ECC203	Analog and Digital CMOS VLSI Design Lab
7.	23ECC204	Microcontrollers and Programmable Digital Signal Processors Lab
8.	23ECC208	IoT and RTOS based Embedded System Design Lab
9.	23ECC209	RTL Synthesis, Simulation and Verification Lab
10.	23ECC210	Mini Project
11.	23ECC211	Industrial Project / Dissertation Phase I
12.	23ECC212	Industrial Project / Dissertation Phase II
PROGRAM ELECTIVE COURSES		
Program Elective – I Courses		
1.	23ECE201	Low Power VLSI
2.	23ECE202	MEMS and Applications
3.	23ECE203	Programming Languages for Embedded Software
Program Elective – II Courses		
4.	23ECE204	Advanced Computer Organization
5.	23ECE205	Algorithms for VLSI Design
6.	23ECE206	System Design with Embedded Linux
Program Elective – III Courses		
7.	23ECE207	Industrial Internet of Things
8.	23ECE208	Semiconductor Device Modeling
9.	23ECE209	VLSI Signal Processing
Program Elective – IV Courses		
10.	23ECE210	Memory Technologies
11.	23ECE211	Physical Design Automation
12.	23ECE212	SoC Design
Program Elective – V Courses		
13.	23ECE213	Nanomaterials and Nanotechnology
14.	23ECE214	Reconfigurable Computing Systems
15.	23ECE215	Unix & Scripting Languages
MANDATORY COURSE		
1.	23MEM103	Research Methodology and IPR

AUDIT COURSES		
1.	23CEA101	Disaster Mitigation And Management
2.	23EGA101	English for Research Paper Writing
3.	23EGA102	Constitution of India
4.	23ADA101	Pedagogy Studies
5.	23EGA104	Personality Development through Life's Enlightenment Skills.
6.	23EEA101	Sanskrit for Technical Knowledge
7.	23EGA103	Stress Management by Yoga
8.	23ECA101	Value Education
OPEN ELECTIVE COURSES		
1.	23CSO101	Business Analytics
2.	23MEO103	Composite Materials
3.	23CEO101	Cost Management of Engineering Projects
4.	23MEO101	Industrial Safety
5.	23MEO102	Introduction to Optimization Techniques
6.	23EEO101	Waste to Energy

23ECC201

ANALOG AND DIGITAL CMOS VLSI DESIGN

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Analog and Digital Design concepts.

COURSE OBJECTIVES: This course aims to
1. Educate about the different Models of MOSFET, so that it can be used in analytical analysis and modelling of the circuits.
2. Demonstrate the construction, analysis and design of basic circuits of Analog IC Design.
3. Demonstrate the construction, analysis and design of basic circuits of Digital IC Design.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Choose and apply appropriate MOS model for analytical modelling/analysis of the circuits.
2. Choose appropriate amplifier or current mirror circuit for a given application or specification.
3. Design various types of amplifiers, Op-Amps and current sources as per the required specifications.
4. Design and analyze any combinational circuits for a given application.
5. Design and analyze sequential circuits for any given application.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	2	3	3	3
CO 2	3	2	3	3	3
CO 3	3	2	3	3	3
CO 4	3	2	3	3	3
CO 5	3	2	3	3	3

UNIT – I

MOS Modelling: Basic MOS Device Physics: MOS structure, MOS I/V Characteristics: Threshold Voltage, Band-Bending, Derivation of I/V Characteristics, Second Order Effects, MOS Device Layout, MOS Device Capacitances, MOS Low Frequencies Small Signal Models, Long Channel vs Short Channel, Latch-up.

Single Stage Amplifiers: Basic Concepts, Common Source Stage: with Resistive Load, Current Source Load, Triode Load, with Source Degeneration, Source Follower, Common Gate Stage, Cascode Stage, Folded Cascode.

UNIT – II

Current Mirrors: Basic Current Mirrors, Cascode Current Mirrors, Wide-Swing Current Mirrors, Wilson and Wildar Current Mirrors.

Frequency Response of Single Stage Amplifiers: Miller Effect, Association of Nodes with Poles, Frequency Response of Single Stage Amplifiers: CS Stage, Source Follower, Common Gate Stage, Cascode Amplifier.

Noise: Statistical Characteristics of Noise: Noise Spectrum, Amplitude Distribution, Correlated and Uncorrelated Sources, Types of Noise: Flicker Noise and Thermal Noise, Representation of Noise in Circuits, Noise in Common Source Amplifier.

UNIT – III

Differential Amplifiers: Single Ended vs Differential Amplifiers, Basic Differential Pair, Analysis of Basic Differential Pair, Common Mode Response, Differential Pair with MOS Load. Frequency Response of Differential Amplifier, Noise in Differential Amplifier.

Operational Amplifiers: One Stage Op-Amp, Two Stage Op-Amp, Gain Boosting, Common Mode Feed-Back, Input Range Limitations, Slew Rate, PSRR.

Stability and Frequency Compensation: General Considerations, Multi-Pole System, Phase Margin, Frequency Compensation, Compensation of Two Stage Op-Amp, Slewing in Two Stage Op-Amp, Compensation Techniques. Typical Design Procedure for 2-Stage Op-Amp.

UNIT – IV

CMOS-Inverter: MOS Static Behavior, Inverter: Static CMOS Inverter, Switching Threshold and Noise Margin Concepts and Their Evaluation of Dynamic Behavior, Power Consumption, Static and Dynamic ESD Protection-Human Body Model.

UNIT – V

Combinational Logic: Static CMOS Design, Logic Effort, Ratioed Logic, Pass Transistor Logic, Dynamic Logic Speed and Power Dissipation in Dynamic Logic, Cascading Dynamic Gates, CMOS Transmission Gate Logic. Sequential Logic: Static Latches and Registers, MUX Based Latches, Static SR Flip-Flops, Master-Slave Edge-Triggered Register, Dynamic Latches, and Registers.

TEXT BOOKS:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill. 2002.
2. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd edition 2003.

SUGGESTED READING:

1. David Johns, Ken Martin, "Analog Integrated Circuit Design", John Wiley & sons. 2004.
2. Jacob Baker.R.et.al., "CMOS Circuit Design", IEEE Press, Prentice Hall, India, 2000.
3. Paul. R. Gray & Robert G. Major, "Analysis and Design of Analog Integrated Circuits", John Wiley & sons. 2004.
4. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH, 3rdEdition 2003.

23ECC202

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Microprocessor and its interfacing, Digital Signal Processing.

COURSE OBJECTIVES: This course aims to
1. Learn about ARM Cortex M4 Microcontroller Architecture Features.
2. Understand the ARM Programming for various applications.
3. Study the DSP fixed and floating processor fundamentals and its development tools.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Compare and select ARM processor core based on requirements of embedded application.
2. Analyse various features of ARM Cortex-M4 Series processor.
3. Develop the skills to program ARM CortexM4 processors.
4. Design interfacing applications on ARM Cortex M4 based microcontroller.
5. Apply various signal processing applications on DSP processor-based platforms.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	1	1	1	3
CO 2	3	1	1	2	1
CO 3	2	1	1	1	1
CO 4	2	1	1	1	3
CO 5	3	1	1	3	3

UNIT – I

Background of ARM: A Brief History, Architecture Versions, Processor Naming, Instruction set development, The Thumb 2 Technology.

The Cortex-M4 Processor: CPU Block diagram, Programming Model- Processor modes, Stacks, Register map, Memory model, Exceptions and Interrupts, Data types, CMSIS (Cortex Microcontroller Software Interface Standard).

UNIT – II

Cortex-M4 Instruction Set: Memory Access Instructions, Data Processing Instructions, Multiply and Divide Instructions, Saturating Instructions, Packing and Unpacking Instructions, Bit Field Instructions, Branch and Control Instructions, Floating Point Instructions, Miscellaneous Instructions.

UNIT – III

Coriex-M4 Peripherals: Nested Vectored Interrupt Controller (NVIC), System Control Block, System Timer-Systick, Memory Protection Unit (MPU), Floating Point Unit (FPU).

UNIT – IV

Cortex- M4 Microcontroller: Tiva C Series TM4C123G ARM Cortex M4 Microcontroller Features, Specifications. Peripherals - Gpios, General Purpose Timers, Watchdog Timers, ADC, Comparators, PWM, Overview of Serial Communication Protocols –UARTS, SSI, I2C, CAN.

UNIT – V

TMS320C67XX: Features of C67XX Processors, Internal Architecture, Functional Units and Operation, Data Paths, Cross Paths, Control Register File, Addressing Modes, Fixed Point Instructions, Conditional Operations, Parallel Operations, Floating Point Instructions.
Application Development Tools: Code Composer Studio (CCS), Application Programs using Filters.

TEXT BOOKS:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3 and Cortex-M4 Processors", Elsevier, 2014.
2. Tiva™ TM4C123GH6PM Microcontroller Reference Manual, 2014.
3. TMS320C67x/C67x+ DSP CPU and Instruction Set Reference Guide, 2006.

SUGGESTED READING:

1. Mark Fisher, "ARM Cortex M4 Cookbook", PACKT Publishing, 2016.
2. ARM Cortex M4 Devices – Generic User Guide, 2010.

23ECC205

IoT AND RTOS BASED EMBEDDED SYSTEM DESIGN

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Computer Architecture, Microprocessors and Microcontrollers.

COURSE OBJECTIVES: This course aims to
1. Understand the overview of Internet of Things, building blocks of IoT and the real-world applications.
2. Analyze the IoT Physical Devices and End Points and Case studies illustrating IoT design.
3. Know the importance of hard/soft Real-Time Systems and to familiarize the cases for tasks, semaphores, queues, pipes, and event flags.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Understand the terminology, enabling technologies and tools of IoT.
2. Develop the building blocks of IoT physical devices and end points using Raspberry Pi and data analytics.
3. Design methodology and case study illustration of different application domains.
4. Analyze various scheduling algorithms and application to real time systems.
5. Illustrate the concepts of real time operating system and VxWorks.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	1	2	2	2	1
CO 2	1	2	2	2	1
CO 3	1	2	2	2	1
CO 4	2	2	2	2	1
CO 5	2	2	2	3	1

UNIT – I

Introduction to Internet of Things: Definitions & Characteristics of IoT, Physical and Logical Design of IoT, IoT Functional Blocks, IoT Communication Models, IoT Communication APIs, IOT Levels & Deployment Templates.

Tools for IoT: Chef, Chef case studies, Puppet, Puppet case study, NETCONF-YANG case studies.

UNIT – II

IoT Physical Devices and End Points: Basic Building Blocks of an IoT Device, Raspberry Pi- about the Raspberry Pi Board, Raspberry Pi Interfaces-Serial, SPI and I2C. Introduction to Beagle Bone Black Board and its Internals.

Data Analytics For IoT: Apache Hadoop, Using Hadoop Map Reduce for Batch Data Analysis, Apache Oozie, Apache Spark, Apache Storm, using Apache Storm Real Time Data Analysis.

UNIT – III

IoT Platforms Design Methodology: IoT Design Methodology, Case Study on IoT System for Weather Monitoring.

Case Studies illustrating IoT Design: Home Automation, Smart Parking, Weather Monitoring System, Weather Reporting Bot, Air Pollution Monitoring, Forest Fire Detection, Smart Irrigation, IoT Printer.

UNIT – IV

RTOS Concepts: Differences between Traditional OS and RTOS, Real Time System Concepts, Hard Versus Soft Real- Time Systems: Examples, Jobs & Processors, Hard and Soft Timing Constraints, Hard Real –Time Systems,

Soft Real Time Systems. Classical Uniprocessor Scheduling Algorithms –RMS, Preemptive EDF, Allowing for Preemptive and Exclusion Condition.

UNIT – V

Introduction to Vx-Works : RTOS Kernel & Issues in Multitasking Task Assignment, Task Switching, Foreground ISRs And Background Tasks, Critical Section, Vxworks – POSIX Real Time Extensions, Timeout Features, Task Creation, Semaphores (Binary, Counting), Mutex, Mailbox, Message Queues. Case Study: Automatic Vending Machine for ESD.

TEXT BOOKS:

1. Arshdeep Bahga and Vijay Madisetti, “Internet of Things - A Hands-on Approach, Universities Press", 2015.
2. Jane W.S.Liu, “Real Time Systems”, Pearson Education, Asia, 2018.
3. Wind River Systems Inc., “VxWorks Programmers Guide”, 2019.

SUGGESTED READING:

1. C.M.Krishna and G.Shin, “Real Time Systems”, McGraw-Hill Companies Inc., 2015.

23ECC206

VLSI DESIGN, VERIFICATION AND TESTING

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Knowledge of Analog and Digital CMOS VLSI Design, C and C++ Language concepts.

COURSE OBJECTIVES: This course aims to
1. The concepts of verification and testing.
2. Data types and OOPs concepts.
3. Randomization in System Verilog.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Familiarity of front-end design and verification and testing and create reusable test environments.
2. Understanding various data types used in System Verilog.
3. Demonstrating OOPs concepts.
4. Make use of Randomization in System Verilog.
5. Verify increasingly complex designs more efficiently and effectively.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	2	2	2	1
CO 2	3	1	2	3	1
CO 3	3	1	2	3	1
CO 4	3	1	2	2	1
CO 5	3	1	2	3	1

UNIT – I

Verification Guidelines: Verification Process, Basic Test Bench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Test Bench Components, Layered Test Bench, Building Layered Test Bench, Simulation Environment Phases, Test Bench Performance.

Data Types: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Creating New Types With Typedef, Creating User-Defined Structures, Type Conversion, Enumerated Types, Constants Strings. Procedural Statements and Routines: Procedural Statements, Tasks, Functions and Void Functions.

UNIT – II

Basic OOPS: Introduction, First Class, Define a Class, OOP Terminology, Creating New Objects, Object De-Allocation, Using Objects, Static Variables Vs. Global Variables, Class Methods, Defining Methods Outside of the Class, Scoping Rules, Using One Class Inside Another.

UNIT – III

Connecting the Test Bench And Design: Separating the Test Bench and Design, Interface Constructs, Stimulus Timing, Interface Driving and Sampling, Connecting it all Together, Top-Level Scope Program Module Interactions. System Verilog Assertions, Understanding Dynamic Objects, Copying Objects.

UNIT – IV

Randomization: Introduction, What to Randomize, Randomization in System Verilog, Constraint Details Solution Probabilities, Controlling Multiple Constraint Blocks, Valid Constraints, In-Line Constraints, The Pre Randomize and Post Randomize Functions, Random Number Functions, Constraints Tips and Techniques, Common Randomization Problems, Iterative and Array Constraints.

UNIT – V

Simulation Based Verification and Testing: Fault Simulation: Parallel, Deductive, Concurrent, Functional Testing Methodologies: Exhaustive Testing, Pseudo-Exhaustive Testing, Structure based Testing: Fault Model based Testing, Stuck-at Faults, Bridging Faults, Stuck-Open Faults, Delay Faults , Fault Grading, Automatic Test Pattern Generation Algorithms: D-Algorithms, PODEM, FAN, etc Design for Testability Methods: Testable Combinational / Sequential Circuits, Scan Path Design, Partial Scan, Built-In Self-Test (BIST), Data Compaction Techniques**.**

TEXT BOOKS:

1. Chris Spears, "System Verilog for Verification", Springer, 2nd Edition 2006.
2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers 2002.
3. Bergeron, Janick. Writing test benches using System Verilog, 1st Edition, Springer Science & Business Media, 2007.

SUGGESTED READING:

1. Writing test benches using System Verilog by Janick Bergeron Edition: illustrated Published by Birkhäuser, 2006, ISBN 0387292217, 9780387292212.
2. System Verilog for Verification: A Guide to Learning the Test bench Language Features by Chris Spear Edition: 2, Published by Springer, 2008 ISBN 0387765298, 9780387765297.
3. Vijayaraghavan, Srikanth, and Meyyappan Ramanathan. A practical guide for System Verilog assertions, Springer Science & Business Media, 2006.

23ECC207

MIXED SIGNAL AND RF IC DESIGN

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Network Theory, Analog Electronics, Analog CMOS VLSI Design.

COURSE OBJECTIVES: This course aims to

1. Introduce students the concept of tuned circuit, matching network, reflection coefficients, transmission lines and MOS high frequency behavior etc.
2. Demonstrate design of High Frequency Amplifiers.
3. To understand the working of Mixed Signal Circuits.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Measure the performance metric of a given RF systems.
2. Understand the design of High bandwidth and LNA circuits.
3. Apply techniques for designing amplifiers for high frequencies.
4. Design and Analyze Nyquist Data converter.
5. Design and Analyze of over-sample Data converter.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	3	2	3	3
CO 2	3	2	3	3	3
CO 3	3	2	3	3	3
CO 4	3	2	3	3	3
CO 5	3	2	3	3	3

UNIT – I

Nonlinearity And Reflection Coefficient: Nonlinearity and Time Variance of System, Effects of Non-Linearity: Harmonic Distortion, Gain Compression, Cross Modulation, Inter-Modulation, Cascaded Non-Linear Stages, **AM-PM Conversion, Device Noise:** Thermal Noise, Flicker Noise Review, Representation of Noise in Circuits **Noise:** Noise as a Random Process, Noise Spectrum, Effect of Transfer Function on the Noise, Sensitivity and Dynamic Range, Passive Impedance Transformation: Q, Series to Parallel Conversion, Scattering Parameters, Review of MOS Device Physics.

UNIT – II

High Frequency Amplifier Design: Bandwidth Estimation using Open-Circuit Time Constants, Bandwidth Estimation using Short-Circuit Time Constants, Rise-Time, Delay and Bandwidth, Zeros to Enhance Bandwidth, Shunt-Series Amplifiers, Tuned Amplifiers, Cascaded Amplifiers, Noise Figure, Intrinsic MOS Noise Parameters. **Low Noise Amplifiers:** General Considerations, Problem of Input Matching, LNA-Topologies – CS-Stage with Inductive Load, CS-Stage with Resistive Feedback, Common Gate Stage, Cascode CS Stage with Inductive De-Generation.

UNIT – III

OP-Amp - As a Comparator, Charge Injection Error, Switched Capacitor Basic Operation and Analysis, First Order Filter, Switched Capacitor Gain Circuits, Sample and Hold Circuit-its Performance.

UNIT – IV

Digital to Analog Converter: Nyquist Rated DAC, Decoder Based Converter, Binary Scaled Converter, Thermometer Coded Converter, Hybrid Converter, Successive Approximation Converter.

Analog To Digital Converter: Algorithmic ADC, Flash Converter, Two-Step ADC, Interpolation ADC, Folding ADC, Piplied ADC, Time Interleaved ADC.

UNIT – V

Oversampled Converter: Oversampling with and without Noise Shaping, System Architecture, Digital Decimation Filter, High Order Modulation, Band Pass Over Sampling Converter, Multi-Bit Oversampling Converter, Third Order ADC.

TEXT BOOKS:

1. Behzad Razavi, "RF Microelectronics", Prentice Hall, 1997**.**
2. Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2004.

SUGGESTED READING:

1. Abidi, P.R. Gray, and R.G. Meyer, eds., "Integrated Circuits for Wireless Communications", New York: IEEE Press, 1999.
2. R. Ludwig and P. Bretchko, "RF Circuit Design, Theory and Applications", Pearson, 2000.

23ECC203

ANALOG AND DIGITAL CMOS VLSI DESIGN LAB

Instruction	3 P Hours per week
Duration of SEE	--
SEE	--
CIE	50 Marks
Credits	1.5

PREREQUISITE: Analog and Digital Design concepts.

COURSE OBJECTIVES: This course aims to
1. Use MOSFET in the design of Analog and Digital Circuits.
2. Design and simulate Digital Circuits.
3. Design and simulate Analog Circuits.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Characterize MOSFET by simulation and extract design parameters.
2. Design and simulate basic digital circuits.
3. Design, simulate and compare single stage amplifiers.
4. Design, simulate and compare differential amplifiers and op-amps.
5. Develop layout of any given circuit.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	3	3	3	3
CO 2	3	3	3	3	3
CO 3	3	3	3	3	3
CO 4	3	3	3	3	3
CO 5	3	3	3	3	3

LIST OF EXPERIMENTS:
1. Characteristics of MOSFET.
2. Calculation of rise time and fall time for CMOS inverter.
3. To build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.
4. Static and Dynamic latches.
5. NMOS Common Source Amplifier.
6. Design of Differential Amplifier.
7. Design of Operational Amplifier.
8. Draw the layout of Inverter Circuit.

ACTIVITY:
Design, simulate and develop layout of a fairly complex transistor level circuit design with a clear and validated specifications.

SUGGESTED READING:
1. Cadence Design Systems (Ireland) Ltd., “Cadence manual”, 2013.

23ECC204

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB

Instruction	3 P Hours per week
Duration of SEE	--
SEE	--
CIE	50 Marks
Credits	1.5

PREREQUISITE: Programming in 'C' and basics of ARM Microcontroller and Digital Signal Processing.

COURSE OBJECTIVES: This course aims to
1. Write the ARM 'C' programming for applications.
2. Understand the interfacing of various modules with ARM Cortex-M4 Microcontroller.
3. Develop assembly and C Programming for DSP processors.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Install, configure, and utilize tool sets for developing applications based on ARM processor core.
2. Design and develop the ARM Cortex M4 based embedded systems for various applications.
3. Develop application programs on ARM and DSP development boards both in assembly and C.
4. Design and implement the digital filters on DSP 67XX processor.
5. Analyse the hardware and software interaction and integration.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	1	3	1	1
CO 2	2	1	3	1	1
CO 3	2	1	3	1	1
CO 4	2	1	3	1	1
CO 5	2	1	3	1	3

LIST OF EXPERIMENTS:

Part A

Experiments to be carried out on Tiva C Series TM4C123G ARM Cortex M4 Microcontroller starter kit.
1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real-time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a micro-phone and display sound levels on LEDs.

Part B

Experiments to be carried out on DSP C67XX evaluation kits and using Code Composer Studio (CCS)
1. To develop assembly code and study the impact of parallel, serial and mixed execution.
2. To develop assembly and C code for implementation of convolution operation.
3. To design and implement HR filters in assembly and in C to enhance the features of given input sequence/signal.
4. To design and implement FIR filters in assembly and in C to enhance the features of given input sequence/signal.

TEXT BOOKS:

1. Tiva™ TM4C123GH6PM Microcontroller Reference Manual, 2014.
2. TMS320C6748™ Fixed- and Floating-Point DSP datasheet, 2017.

SUGGESTED READING:

1. Mark Fisher, "ARM Cortex M4 Cookbook", PACKT Publishing, 2016.
2. TMS320C67x/C67x+ DSP CPU and Instruction Set Reference Guide, 2006.

23ECC208

IoT AND RTOS BASED EMBEDDED SYSTEM DESIGN LAB

Instruction	3 P Hours per week
Duration of SEE	--
SEE	--
CIE	50 Marks
Credits	1.5

PREREQUISITE: Embedded Systems.

COURSE OBJECTIVES: This course aims to
1. Implement hardware setup for IoT and interface the components to perform applications.
2. Develop basic programming skills for deploying various IoT protocols.
3. Develop the RTOS based programming skills for embedded systems.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Analyze various software and hardware components required for IoT technology.
2. Interface analog and digital sensing & actuating equipment using Raspberry Pi.
3. Apply knowledge of IoT to solve engineering problems.
4. Understand the programming concepts of RTOS.
5. Analyze Multitasking, IPC and scheduling concepts.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	2	2	2	2
CO 2	2	2	2	2	2
CO 3	2	2	2	2	2
CO 4	2	2	2	2	1
CO 5	2	2	2	3	1

LIST OF EXPERIMENTS:
1. Familiarize about the Raspberry Pi hardware and to perform necessary software installation.
2. To interface LED/Buzzer with Raspberry Pi and write a program to turn On LED for 1 sec after every 2 seconds.
3. To interface Push Button/Digital sensor (IR/LDR) with Raspberry Pi and write a program to turn ON LED when push button is pressed or at sensor detection.
4. To interface DHT11 sensor with Raspberry Pi and write a program to print temperature and humidity readings.
5. Write a program on Raspberry Pi to upload/retrieve temperature and sensor data from Thingspeak cloud.
6. Write a program on Beaglebone Black to publish and subscribe sensor data to/from MQTT broker.
7. Introduction to RTOS (VxWorks) and its basic functions.
8. RTOS Timer programming (VxWorks).
9. RTOS Task function programming (VxWorks).
10. Multitasking using round robin scheduling.
11. IPC using message queues.
12. IPC using semaphore.
13. IPC using mail box.

SUGGESTED READING:
1. Practical Python Programming for IoT: Build advanced IoT projects using a Raspberry Pi 4, MQTT, RESTful APIs, WebSockets, and Python 3 Paperback – Import, 12 November 2020.
2. Silberschatz, Galvin, Gange “Operating Systems Concepts” 8/e, Wiley Education, 2018.
3. Wind River Systems Inc., “VxWorks Programmers Guide”, 2019.

23ECC209

RTL SYNTHESIS, SIMULATION AND VERIFICATION LAB

Instruction	3 P Hours per week
Duration of SEE	--
SEE	--
CIE	50 Marks
Credits	1.5

PREREQUISITE: Digital Design and Verilog HDL programming skills.

COURSE OBJECTIVES: This course aims to
1. The simulation of combinational and sequential circuits.
2. FSM based designs.
3. Implementation of DFT and FFTs.
4. Verify layout of basic digital circuits.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Demonstrate the process steps required for simulation /synthesis.
2. Design and simulate various combinational and sequential circuits using HDL.
3. Develop an RTL code for various real time applications.
4. Synthesize / Simulate an RTL code for several digital designs.
5. Build and verify various digital circuits.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	1	1	3	1
CO 2	2	1	1	3	1
CO 3	2	1	1	3	1
CO 4	2	1	1	3	1
CO 5	2	1	1	3	1

LIST OF EXPERIMENTS:
1. Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator,
2. Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, Bidirectional) 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
3. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
4. Vending machines - Traffic Light controller, ATM, Elevator control.
5. PCI Bus & arbiter and downloading on FPGA.
6. UART/ USART implementation in Verilog.
7. Realization of single port SRAM in Verilog.
8. Verilog implementation of Arithmetic circuits like serial adder / subtractor, parallel adder/ subtractor, serial/parallel multiplier.
9. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.
10. FIR/IIR filter implementation in Verilog.

SUGGESTED READING:
1. Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall 2003.
2. Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx, 2011.
3. Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books, 2002.

23ECC210

MINI PROJECT

Instruction	2 P Hours per Week
Duration of SEE	--
SEE	--
CIE	50 Marks
Credits	1

PREREQUISITE: Knowledge of preparing slides by using power point presentations, Capable of searching for suitable literature and Presentation skills.

COURSE OBJECTIVES: This course aims to

1. The student takes up investigative study in the broad field of Engineering / Technology, either fully theoretical/practical or involving both theoretical and practical.
2. The work to be assigned by the Department on an individual basis or two/three students in a group, under the guidance of a supervisor.
3. This is expected to provide a good initiation for the student(s) towards R&D.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Formulate a specific problem and give a solution.
2. Develop model/models theoretical/practical/numerical form.
3. Solve, interpret/correlate the results and discussions.
4. Conclude the results obtained.
5. Write the documentation in standard format.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	1	3	3	1
CO 2	3	1	3	3	1
CO 3	3	1	3	3	2
CO 4	3	2	3	3	1
CO 5	3	3	2	2	2

GUIDELINES:

- As part of the curriculum in the II- semester of the Program each students shall do a mini project, generally comprising about three to four weeks of prior reading, twelve weeks of active research, and finally a presentation of their work for assessment.
- Each student will be allotted to a faculty supervisor for mentoring.
- Mini projects should present students with an accessible challenge on which to demonstrate competence in research techniques, plus the opportunity to contribute something more original.
- Mini projects shall have inter disciplinary/ industry relevance.
- The students can select a mathematical modeling based/Experimental investigations or Numerical modeling.
- All the investigations are clearly stated and documented with the reasons/explanations.
- The mini-project shall contain a clear statement of the research objectives, background of work, literature review, techniques used, prospective deliverables, detailed discussion on results, conclusions and references.

DEPARTMENT COMMITTEE: SUPERVISOR AND TWO FACULTY COORDINATORS

Guidelines for awarding marks (CIE):	Max. Marks: 50	
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	20	Progress and Review
	05	Report
Department Committee	05	Relevance of the Topic
	05	PPT Preparation
	05	Presentation
	05	Question and Answers
	05	Report Preparation

23ECC211

INDUSTRIAL PROJECT / DISSERTATION PHASE I

Instruction	20 P Hours per Week
Duration of SEE	--
SEE	--
CIE	100 Marks
Credits	10

PREREQUISITE: Capable of carrying out suitable literature survey and accomplish/execute a software/hardware based project in Embedded, VLSI and allied areas.

COURSE OBJECTIVES: This course aims to

1. The 'Industrial project/Dissertation Phase 1(Project work) will preferably be a problem with research potential and should involve scientific research, design, generation/collection and analysis of data, determining solution and must preferably bring out the student contribution(s).
2. To expose and learn the required simulation software/experimental techniques.
3. To carry out the work in a research environment or in an industrial environment.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Ability to synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem.
2. Learn the required software/ computational/analytical tools for implementations.
3. Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design.
4. Ability to present the findings of their technical solution in a written report.
5. Presenting the work in International/ National conference or reputed journals.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	3	3	3	1
CO 2	3	3	3	3	2
CO 3	3	3	3	3	2
CO 4	3	3	2	3	1
CO 5	2	2	2	3	2

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have the following.

- Relevance to social needs of society.
- Relevance to value addition to existing facilities in the institute.
- Relevance to industry need.
- Problems of national importance.
- Research and development in various domain.

The student should complete the following:

- Literature survey Problem Definition.
- Motivation for study and Objectives.
- Preliminary design / feasibility / modular approaches.
- Implementation and Verification.
- Report and presentation.

As per the AICTE and Institute directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e., Phase – I and Phase – II.

Guidelines for Dissertation Phase – I:

- The dissertation may be carried out preferably in-house i.e., departments laboratories and centers OR in industry allotted through departments T & P coordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Embedded and VLSI domains. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.
- Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.
- Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
- Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.

Guidelines for awarding	Marks in CIE:	Max. Marks: 100
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	30	Project Status / Review(s)
	20	Report
Departmental Review Committee	10	Relevance of the Topic
	10	PPT Preparation(s)
	10	Presentation(s)
	10	Question and Answers
	10	Report Preparation

Note: Departmental Review committee has to assess the progress of the student for every two weeks.

23ECC212

INDUSTRIAL PROJECT / DISSERTATION PHASE II

Instruction	32 P Hours per Week
Duration of SEE	Viva - Voce
SEE	100 Marks
CIE	100 Marks
Credits	16

PREREQUISITE: Should have completed literature survey and defined problem statement with a brief idea of the methodology, as a part of Industrial Project/ Dissertation Phase-I.

COURSE OBJECTIVES: This course aims to
1. Industrial project/Dissertation Phase 2 is the continuation of Industrial project/Dissertation Phase 1
2. Implementation of Project objectives.
3. Presentation of periodic reviews of the objectives and preparing of Dissertation in a prescribed format.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Ability to synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem.
2. Learn the required software/ computational/analytical tools for implementations.
3. Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design.
4. Ability to present the findings of their technical solution in a written report.
5. Presenting the work in International/ National conference or reputed journals.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	3	2	3	2
CO 2	3	3	3	3	2
CO 3	3	3	3	3	2
CO 4	3	3	3	3	2
CO 5	3	2	2	2	2

As per the AICTE and Institute directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I. and Phase – II.

SYLLABUS CONTENTS:
- The dissertation may be carried out preferably in-house i.e. departments laboratories and centers OR in industry allotted through departments T & P coordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Embedded and VLSI domains.
- In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.

GUIDELINES FOR DISSERTATION PHASE – II:
The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be based on:
- Experimental verification / Proof of concept.
- Design, fabrication, testing of Communication System.
- The viva-voce examination will be based on the above report and work.

During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.

- Phase – II deliverables: A dissertation report as per the specified format, developed system in the form of hardware and/or software, A record of continuous progress.
- Phase – II evaluation: Guide along with appointed external examiner shall assess the progress / performance of the student based on report, presentation and Q & A.
- In case of unsatisfactory performance, committee may recommend for extension or repeating the work.

Guidelines for awarding marks in CIE: Max. Marks: 100		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Departmental Review Committee	05	Review 1
	10	Review 2
	10	Review 3
	15	Final presentation with the draft copy of the report
	10	Submission of the report in a standard format
Supervisor	10	Regularity and Punctuality
	10	Work Progress
	10	Quality of the work which may lead to publications
	10	Analytical / Programming / Experimental Skills Preparation
	10	Report preparation in a standard format

Guidelines for awarding marks in SEE: Max. Marks: 100		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
External and Internal Examiner(s) together	20	Power Point Presentation
	40	Quality of thesis and evaluation
	20	Quality of the project • Innovations • Applications • Live Research Projects • Scope for future study • Application to society
	20	Viva-Voce

Note: Departmental Review committee has to assess the progress of the student for every two weeks

23ECE201

LOW POWER VLSI

(Program Elective - I)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Students should have prior knowledge of Analog and Digital CMOS VLSI Design.

COURSE OBJECTIVES: This course aims to

1. Know the sources of power dissipation and need for low power designs for emerging technologies.
2. Understand the concepts of Low power design techniques for digital circuits.
3. Analyze the power dissipations of memory and processor systems and able to adopt suitable methods for power reduction.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Identify and Understand leakage sources and reduction techniques.
2. Understand the impact of power on system performance and reliability.
3. Analyze and apply various low power circuit techniques for combinational and sequential circuits.
4. Explain power minimization techniques for Clock distribution, arithmetic, and memory subsystem.
5. Characterize and model power consumption & understand the basic analysis methods for Microprocessor Design System.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	1	3	2	1
CO 2	3	1	3	2	1
CO 3	3	1	3	3	1
CO 4	2	1	3	2	1
CO 5	3	1	3	3	1

UNIT – I

Technology & Circuit Design Levels: Sources of Power Dissipation in Digital ICs, Degree of Freedom, Recurring Themes in Low-Power, Emerging Low Power Approaches, Dynamic Dissipation in CMOS, Effects of V_{dd} & V_t on Speed, Constraints on V_t Reduction, Transistor Sizing & Optimal Gate Oxide Thickness, Impact of Technology Scaling, Technology Innovations.

UNIT – II

Low Power Circuit Techniques: Power Consumption in Circuits, Flip-Flops & Latches, High Capacitance Nodes, Energy Recovery, Reversible Pipelines, High Performance Approaches.

UNIT – III

Low Power Clock Distribution: Power Dissipation in Clock Distribution, Single Driver versus Distributed Buffers, Buffers & Device Sizing under Process Variations, Zero Skew vs Tolerable Skew, Chip & Package Co-Design of Clock Network.

UNIT – IV

Logic Synthesis for Low Power Estimation Techniques: Power Minimization Techniques, Low Power Arithmetic Components-Circuit Design Styles, Adders, Multipliers. Low Power Memory Design: Sources & Reduction of Power Dissipation in Memory Subsystem, Sources of Power Dissipation in DRAM & SRAM.

UNIT – V

Low Power Microprocessor Design System: Power Management Support, Architectural Tradeoffs for Power, Choosing The Supply Voltage, Low-Power Clocking, Implementation Problem for Low Power, Comparison of Microprocessors for Power & Performance.

TEXT BOOKS:

1. Jan M. Rabaey and MassoudPedram, “Low Power Design Methodologies”, Kluwer Academic, 1996.
2. Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sons, Inc., 2000.

SUGGESTED READING:

1. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley, 1999.
2. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
3. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer, 1995.

23ECE202

MEMS AND APPLICATIONS

(Program Elective - I)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Fundamentals of Semiconductors & Physics.

COURSE OBJECTIVES: This course aims to
1. Integrate the knowledge of semiconductors and solid mechanics to fabricate MEMS devices.
2. Explore the various possible materials and rudiments of Micro fabrication techniques.
3. Identify and understand the mechanism of various sensors and actuators.
4. Introduce various RF MEMS Devices and their applications.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Understand the fundamental concepts of MEMS and Microsystems.
2. Classify and discuss various possible materials for MEMS based devices.
3. Illustrate various process steps involved in fabrication of MEMS devices.
4. Apply knowledge to design micro sensors and micro actuators.
5. Apply knowledge to design RF MEMS devices.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	1	1	1	1	1
CO 2	2	1	1	1	1
CO 3	2	2	3	1	1
CO 4	2	2	3	2	1
CO 5	2	3	3	2	1

UNIT – I

MEMS And Microsystem: Introduction to MEMS, Microsystems and Microelectronics, Multidisciplinary Nature of MEMS, Miniaturization and its Benefits, Scaling Laws in Miniaturization, MEMS Design Considerations, Advantages of MEMS Technology, Applications of MEMS.

UNIT – II

Materials for MEMS: Introduction, Substrates & Wafers, Active Substrate Materials, Silicon as a Substrate Material, Silicon Compounds, Piezoelectric Crystals, Polymers, Packaging Materials.

UNIT – III

Microfabrication: Introduction, Fabrication Process – Wafer Processing, Photolithography, Ion Implantation, Oxidation, Chemical Vapor Deposition (CVD), Physical Vapor Deposition, Deposition By Epitaxy, Etching, Manufacturing Process - Bulk Micromachining, Surface Micromachining and LIGA Process, Packaging Technology, System Level Packaging, Single and Multichip Packaging. Microsystem Packaging, Interfacings in Microsystem Packaging.

UNIT – IV

MEMS Based Sensors and Actuators: Introduction, Working Principles of Microsystem - Micro Sensors, Micro Actuators, MEMS with Micro Sensors: Pressure Sensors, Temperature Sensors, Humidity Sensors, Accelerometers, Gyroscopes, Biomedical Sensors, Chemical Sensors, MEMS with Micro Actuators: Microgrippers, Micromotors, Microgears, Micropumps, Microfluidics.

UNIT – V

RF MEMS Devices: RF MEMS Switches, Mechanical Switches and Electronic Switches for RF and Microwave Applications, Approaches for Low-Actuation-Voltage Switches, RF MEMS Reconfigurable Antennas, RF MEMS Reconfigurable Filters and RF MEMS Phase Shifters.

TEXT BOOKS:

1. Tai-Ran Hsu, MEMS and Microsystems: Design, Manufacture, and Nanoscale Engineering, 2nd Edition, John Wiley & Sons, Inc., Hoboken, New Jersey, 2008.
2. Gabriel M Rebeiz, "RF MEMS - Theory Design and Technology", John Wiley, 2004.
3. Microsystem Design by Stephen D. Senturia, Springer International, Edition, 2010.

SUGGESTED READING:

1. Marc Madou, ―Fundamentals of Micro Fabrication‖ CRC Press.
2. Mohamed Gad-el-Hak, ―The MEMS Handbook‖, CRC Press.
3. Julian W.Gardner, Vijay K.Varadan, Osama O. Awadel Karim, “Micro sensors MEMS and Smart Devices”, John Wiby & sons Ltd., 2001.
4. Iannacci, J. (2013). Practical guide to RF-MEMS. John Wiley & Sons.

23ECE203

PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE

(Program Elective - I)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Embedded systems and C programming.

COURSE OBJECTIVES: This course aims to

1. Introduce students to various programming languages like C, C++, Java script, PERL, etc.
2. Distinguish between Procedural and OOP language, Introduce features of OOPs etc.
3. Demonstrate the development of some typical applications using different Programming languages.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Develop embedded C application of moderate complexity.
2. Summaries the object-oriented programming concepts.
3. Build the Object-Oriented approach to software that models application and Develop algorithms in C++.
4. Understand the overloading and Inheritance concepts of programming.
5. Differentiate interpreted languages from compiled languages.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	1	2	2	1
CO 2	2	1	1	2	1
CO 3	2	1	1	2	1
CO 4	1	1	1	2	1
CO 5	2	1	2	2	1

UNIT – I

Embedded 'C' Programming: Bitwise Operations, Dynamic Memory Allocation, OS Services, Linked Stack and Queue, Sparse Matrices, Binary Tree, Interrupt Handling in C, Code Optimization Issues, Writing LCD Drives, LED Drivers, Drivers for Serial Port Communication, Embedded Software Development Cycle and Methods (Waterfall, Agile).

UNIT – II

Object Oriented Programming: Introduction to Procedural, Modular, Object Oriented and Generic Programming Techniques, Limitations of Procedural Programming, Objects, Classes, Data Members, Methods, Data Encapsulation, Data Abstraction and Information Hiding, Inheritance, Polymorphism.

UNIT – III

CPP Programming: 'C_{in}', 'C_{out}', Formatting and I/O Manipulators, New and Delete Operators, Defining a Class, Data Members and Methods, 'This' Pointer, Constructors, Destructors, Friend Function, Dynamic Memory Allocation.

UNIT – IV

Overloading And Inheritance: Need of Operator Overloading, Overloading the Assignment, Overloading using Friends, Type Conversions, Single Inheritance, Base and Derived Classes, Friend Classes, Types of Inheritance, Hybrid Inheritance, Multiple Inheritance.

Templates: Function Template and Class Template, Member Function Templates and Template Arguments.

UNIT – V

Exception Handling: Syntax for Exception Handling Code: Try-Catch-Throw, Multiple Exceptions.

Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.

PERL: Operators, Statements Pattern Matching Etc. Data Structures, Modules, Objects, Tied Variables, Inter Process Communication Threads, Compilation & Line Interfacing.

TEXT BOOKS:

1. Michael J. Pont, "Embedded C", Pearson Education, 2ndEdition,2008.
2. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999.

SUGGESTED READING:

1. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition2011.
2. Michael Berman, "Data structures via C++", Oxford University Press, 2002.

23ECE204

ADVANCED COMPUTER ORGANIZATION

(Program Elective - II)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Fundamentals of Computer Architecture.

COURSE OBJECTIVES: This course aims to
1. Learn about processor design for computer system.
2. Understand the memory organization of the computer.
3. Study the I/O organization and parallel computer systems.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Analyze the computer arithmetic operations.
2. Design of control unit of the computer.
3. Understand the memory organization of the computer.
4. Interface various I/O modules and various buses to the computer system.
5. Analyze the multiprocessor environment for the computer system.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	1	2	2	1
CO 2	2	1	1	2	1
CO 3	2	1	1	2	1
CO 4	1	1	1	2	1
CO 5	2	1	2	2	1

UNIT – I

Processor Design: Data Representation, Instruction Formats, Data Path Design: Fixed Point Arithmetic and Floating-Point Arithmetic, CPU Organization, Instruction Pipelining, Super Scalar Techniques, Linear Pipeline Processors, Super Scalar and Super Pipeline Design.

UNIT – II

Control Unit Design: Basic Concepts: Basic Control Unit of the Computer System. Hardwired Implementation, Micro- Programmed Control Unit: Basic Concepts, Microinstruction Sequencing: Design Considerations, Sequencing Techniques, Address Generation, Microinstruction Execution, Case Study for Micro-Programmed Control Unit (TI 8800).

UNIT – III

Memory Organization: Internal Memory, Computer Memory System Overview, The Memory Hierarchy, Random Access Memories, Cache Memory, Elements of Cache Design, Virtual Memory- Protection and Examples of Virtual Memory, Replacement Policies.

UNIT – IV

I/O Organization: Accessing I/O Devices, Programmed I-O, Interrupts, DMA, Bus Arbitration; Synchronous Bus and Asynchronous Bus, Interface circuits, Parallel port, Serial Port, Standard I/O Interfaces, IO Processor, PCI Bus, SCSI Bus, USB Bus Protocols.

UNIT – V

Parallel Computer Systems: Instruction Level Parallelism (ILP) – Concept and Challenges, Limitations on ILP, Thread Level Parallelism, Vector Processors (SIMD), Cache Coherence: Write-through Protocol and Write-Back Protocol, Message-Passing Multi-Computers, Multi-Processors – Characteristics, Symmetric and Distributive Shared Memory Architecture.

TEXT BOOKS:

1. Carl Hamacher, Vranesic, Zaky, "Computer Organization", 6thedition, MGH, 2012
2. William Stallings, "Computer Organization and Architecture designing for Performance", 10thedition, PHI, 2016.

SUGGESTED READING:

1. John L. Hennessy and David A. Patterson, "Computer Architecture", A quantitativeApproach, 6th Edition, Elsevier, 2017.
2. Hayes John P, "Computer Architecture and organization" 3rd Edition, MGH, 1998.

23ECE205

ALGORITHMS FOR VLSI DESIGN

(Program Elective - II)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Basics of VLSI.

COURSE OBJECTIVES: This course aims to:

1. Understand the concepts of Physical Design Process such as partitioning, Floor planning Placement and Routing.
2. Discuss the concepts of design optimization algorithms and their application to physical design automation.
3. Understand the concepts of simulation and synthesis in VLSI Design.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Describe and formulate the flow of VLSI Design for any application.
2. Explain the algorithms for floor planning, placement and routing the digital designs at frontend level & at backend VLSI Design level.
3. Compare the various global routing algorithms, ILP approaches.
4. Analyze single layer and three-layer detailed routing algorithms.
5. Apply cell routing and minimization techniques, 1D and 2D compactions.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	1	1	1	1
CO 2	1	3	3	2	3
CO 3	1	2	2	2	2
CO 4	2	2	1	3	2
CO 5	1	3	3	2	2

UNIT – I

Logic Synthesis & Verification

Introduction to Combinational Logic Synthesis, Binary Decision Diagram, Hardware Models for High-Level Synthesis.

Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing & Evolution, other Partitioning Algorithms.

UNIT – II

Placement, Floor Planning & Pin Assignment: Problem Formulation, Simulation Base Placement Algorithms, other Placement Algorithms, Constraint-Based Floor Plannning, Floor Planning Algorithms for Mixed Block & Cell Design. General & Channel Pin Assignment.

UNIT – III

Global Routing: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithm, Line Probe Algorithm, Steiner Tree based Algorithms, ILP based Approaches.

UNIT – IV

Detailed Routing: Problem Formulation, Classification of Routing Algorithms, Single Layer Routing Algorithms, Two Layer Channel Routing Algorithms, Three Layer Channel Routing Algorithms, and Switchbox Routing Algorithms.

UNIT – V

Over The Cell Routing & Via Minimization: Two Layers over the Cell Routers, Constrained & Unconstrained Via Minimization.

Compaction: Problem Formulation, One-Dimensional Compaction, Two Dimension - based Compaction, Hierarchical Compaction.

TEXT BOOKS:

1. Naveed Shervani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publisher, Second edition.
2. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.

SUGGESTED READING:

1. Rolf Drechsheler: "Evolutionary Algorithm for VLSI", Second edition.
2. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002.

23ECE206

SYSTEM DESIGN WITH EMBEDDED LINUX

(Program Elective - II)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Fundamentals of Computer Organization and Architecture, Embedded Systems.

COURSE OBJECTIVES: This course aims to

1. Introduction student to the need of Embedded Linux and to differentiate between desktop and embedded Linux.
2. Introduce students to different board support packages and divers for embedded Linux.
3. Demonstrate embedded Linux development cycle and use of memory management.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Understand the importance of Embedded Linux in system design.
2. Analyze the architecture of embedded Linux in detail.
3. Explain the Linux BSP for a hardware platform.
4. Develop and Debug the drivers in Embedded Linux.
5. Apply the concepts of μC Linux to system design.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	1	1	1	3	1
CO 2	2	1	2	3	1
CO 3	3	1	2	2	1
CO 4	3	2	2	2	1
CO 5	2	2	2	3	1

UNIT – I

Introduction: Need of Embedded Linux, Embedded Linux versus Desktop Linux, Embedded Linux Distributions Embedded Linux Architecture, Kernel Architecture: Hardware Abstraction Layer (HAL), Memory Manager, Scheduler, File System, IO Subsystem, Networking Subsystems, IPC; User Space, Linux Start-Up Sequence.

UNIT – II

Board Support Package: Inserting BSP In Kernel Build Procedure, The Boot Loader Interface, Memory Map, Interrupt Management, The PCI Subsystem, Timers, UART, and Power Management. Embedded Storage: Flash Map, Memory Technology Device, MTD Architecture, Embedded File Systems.

UNIT – III

Embedded Drivers: Linux Serial Driver, Ethernet Driver, And I2C Subsystem on Linux, USB Gadgets, Watchdog Timer, And Kernel Modules. Porting Applications: Architectural Comparison, Application Porting Roadmap.

UNIT – IV

Real-Time Linux: Linux and Real-Time: Building and Debugging: Building the Kernel, Building the Root File System, Integrated Development Environment, Elementary Concepts of Debugging. Embedded Graphics: Graphics System, Introduction to Display Hardware.

UNIT – V

Uclinux: Linux on MMU - Less Systems, Program Load and Execution, Memory Management, File / Memory Mapping.

TEXT BOOKS:

1. Derek Molloy, “Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux”, Wiley, 1st Edition, 2014.
2. Christopher Hallinan, “Embedded Linux Primer: A Practical Real-World Approach”, Prentice Hall, 2nd Edition, 2010.

SUGGESTED READING:

1. P Raghvan, Amol Lad, SriramNeelakandan, “EmbeddedLinux System Design and Development”, Auerbach Publications, 2005.
2. KarimYaghmour, “Building Linux Systems”, O’Reilly & Associates, 2008.

23ECE207

INDUSTRIAL INTERNET OF THINGS

(Program Elective - III)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Embedded Systems and Internet of Things.

COURSE OBJECTIVES: This course aims to

1. Provide an overview of Industrial Internet of Things and Modeling of CPS and CMS.
2. Introduce Architectural Design Patterns for CMS and IIoT, Artificial Intelligence and Data Analytics for manufacturing.
3. Introduction to Advance manufacturing and Innovation Ecosystems.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Understand the Industrial Internet of Things and Cyber Physical manufacturing.
2. Analyze the Cyber Physical and Cyber Manufacturing systems.
3. Evaluate the Architectural design patterns for industrial Internet of Things.
4. Apply the AI and data Analytics for Industrial Internet of Things.
5. Evaluation of Workforce and Human Machine Interaction and Application of Industrial Internet of Things.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	2	2	2	1
CO 2	2	2	2	2	1
CO 3	2	2	2	2	1
CO 4	2	2	2	2	1
CO 5	2	2	2	2	1

UNIT – I

Understanding Industrial Internet of Things (IIoT): Industrial Internet of Things and Cyber Manufacturing Systems, Application Map for Industrial Cyber Physical Systems, Cyber Physical Electronics Production.

UNIT – II

Modeling of CPS and CMS: Modeling of Cyber Physical Engineering and Manufacturing, Model based Engineering of Supervisory Controllers for Cyber Physical Systems, Evaluation Model for Assessments of Cyber Physical Production Systems.

UNIT – III

Architectural Design Patterns for CMS and IIot: CPS-Based Manufacturing and Industry 4.0., Integration of Knowledge Base Data Base and Machine Vision, Interoperability in Smart Automation, Enhancing Resiliency in Production Facilities through CPS. Communication and Networking of IIot.

UNIT – IV

Artificial Intelligence and Data Analytics for Manufacturing: Application of CPS in Machine Tools, Digital Production, Cyber Physical System Intelligence, Introduction to Big Data, Machine Learning and Condition Monitoring.

Evaluation of Workforce and Human Machine Interaction: Worker and CPS, Strategies to Support user Intervention.

UNIT – V

Introduction to Advance Manufacturing and Innovation Ecosystems:

Application of IIot: Smart Metering, E-Health Body Area Networks, City Automation, Automotive Applications, Home Automation, Smart Cards, Plant Automation, Real Life examples of IIOT in Manufacturing Sector. Industrial IoT - Application Domains: Oil, Chemical and Pharmaceutical Industry, Applications of UAVs in Industries.

TEXT BOOKS:

1. Sabina Jeschke, Christian Brecher Houbing Song, Danda B. Rawat "Industrial Internet of Things Cyber Manufacturing Systems", springer, 2016.
2. Alasdair Gilchrist, "Industry 4.0: The Industrial Internet of Things", Apress, 2017.

SUGGESTED READING:

1. The Internet of Things: Key Applications and Protocols, Olivier Hersent Actility, David Boswarthick ETSI, Omar Elloumi Alcatel-Lucent, 2nd Edition, Wiley Publications. 2012.
2. Internet of Things- From Research and Innovation to Market Deployment; By Ovidiu & Peter; River Publishers Series, 2022.

23ECE208

SEMICONDUCTOR DEVICE MODELLING

(Program Elective - III)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Physics of Semiconductors.

COURSE OBJECTIVES: This course aims to

1. To acquire the fundamental knowledge and to expose to the field of semiconductor theory and devices and their applications.
2. To gain adequate understanding of semiconductor device modelling aspects, designing devices for electronic applications.
3. To acquire the fundamental knowledge of different semiconductor device modelling aspects.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Acquire knowledge about physics involved in modelling of semiconductor device.
2. Explore the properties of PN Junction Diodes.
3. Discuss the device level characteristics of BJT transistors.
4. Modelling of MOSFET devices using MATLAB, SPICE and ATLAS / SYNOPSYS.
5. Summaries various ultra-deep submicron transistor design issues.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	1	1	1	1	3
CO 2	1	1	1	1	3
CO 3	1	2	1	2	2
CO 4	2	3	3	3	3
CO 5	2	3	3	3	3

UNIT – I

Semiconductor Physics: Metals, Insulator, Semiconductors, Intrinsic and Extrinsic Semiconductors, Direct and Indirect Band Gap, Free Carrier Densities, Fermi Distribution, Density of States, Boltzmann Statistics, Thermal Equilibrium, Current Flow Mechanisms, Drift Current, Diffusion Current, Mobility, Band Gap Narrowing, Resistance, Generation and Recombination, Lifetime, Internal Electro-Static Fields and Potentials, Poisson's Equation, Continuity Equations, Drift-Diffusion Equations.

UNIT – II

PN-Junction Diodes: Thermal Equilibrium Physics, Energy Band Diagrams, Space Charge Layers, Internal Electro-Static Fields and Potentials, Reverse Biased Diode Physics, Junction Capacitance, Wide and Narrow Diodes, Transient Behavior, Transit Time, Diffusion Capacitance, Small Signal Model.

UNIT – III

Bipolar Transistors: Basic Theory and Operation, Heavy Doping Effects, Double Diffused Transistors, Ebers-Moll Model, Low Forward Bias, Junction and Diffusion Capacitance, Transit Times, Parasitic, Small-Signal Models, Early Effect, Saturation and Inverse Operation, Breakdown Mechanisms, Punch-through.

UNIT – IV

MOS Transistors: MOS Capacitor, Accumulation, Depletion, Strong Inversion, Threshold Voltage, Contact Potential, Oxide and Interface Charges, Body Effect, Drain Current, Saturation Voltage, Gate Work Function, Channel Mobility, Sub-Threshold Conduction, Short Channel Effects, Effective Channel Length, Effects of

Channel Length and Width on Threshold Voltage, Compact Models for MOSFET and their Implementation in SPICE, Level 1, 2 and 3, MOS Model Parameters in SPICE.

UNIT – V

UDSM Transistor Design Issues: Short Channel and Ultra Short Channel Effects; Effect T_{ox}, Effect of High K and Low K Dielectrics on the Gate Leakage and Source – Drain Leakage; Tunneling effects; Different Gate Structures in UDSM - Impact and Reliability Challenges in UDSM.

TEXT BOOKS:

1. Y.P. Tsividis, The MOS Transistor, McGraw-Hill, international edition ed., 1988.
2. Nandita DasGupta, Amitava DasGupta, Semiconductor Devices: Modelling and Technology, PHI.
3. S.M.Sze, Semiconductor Devices Physics and Technology, John Wiley & Sons Inc, (2/e).

SUGGESTED READING:

1. Getreu, Modeling the bipolar transistor, New York, NY: Elselvier, 1978.
2. D. Roulston, Bipolar Semiconductor Devices, McGraw Hill, 1990.
3. N.Arora, MOSFET Models for VLSI Circuit Simulation, Springer-Verlag, 1993.
4. P.Antognetti and G. Massobrio, Semiconductor Device Modelling with SPICE, McGraw-Hill, 1988.
5. D.W. Greve, Field Effect Devices and Applications, Prentice Hall Series in Electronics and VLSI, 1998.

23ECE209

VLSI SIGNAL PROCESSING

(Program Elective - III)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: VLSI Design, Signals and Systems and DSP concepts.

COURSE OBJECTIVES: This course aims to
1. Understand fundamentals of DSP systems.
2. Impart the knowledge of Pipelined and parallel recursive and adaptive filters.
3. Analyze the Systolic architecture design concepts.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Understand the concepts of various DSP algorithms, its DFG representation, pipelining and parallel processing approaches.
2. Demonstrate retiming techniques and systolic architecture design concepts.
3. Develop various convolution algorithms for programmable hardware.
4. Evaluate pipelining and parallel processing techniques in the design of recursive digital filters.
5. Discuss algorithmic strength reduction techniques and evolution of DSP processors.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	1	3	2	1
CO 2	3	1	3	2	1
CO 3	3	1	3	1	1
CO 4	3	1	2	2	1
CO 5	3	2	3	1	1

UNIT – I

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for Low Power, Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.

UNIT – II

Folding: Introduction – Folding, Transform – Register Minimization Techniques – Register Minimization in Folded Architectures – Folding of Multirate Systems.

UNIT – III

Unfolding: Introduction – an Algorithm for Unfolding – Properties of Unfolding – Critical Path, Unfolding and Retiming – Applications of Unfolding.

UNIT – IV

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, Fir Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

UNIT – V

Fast Convolution: Introduction, Cook, TOOM Algorithm, Winogard Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

TEXT BOOKS:

1. Keshab K. Parthi, "VLSI Digital signal processing systems, design and implementation", Wiley, Inter Science, 1999.

2. Mohammad Isamail and Terri Fiez, "Analog VLSI signal and information processing", McGraw Hill, 1994.
3. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice, Hall, 1985.

SUGGESTED READING:

1. U. Meyer -Baese, Digital Signal Processing with FPGAs, Springer, 2004.
2. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing, Jose E. France, Yannis Tsividis, Prentice Hall, 1994.
3. VLSI Digital Signal Processing, Medisetti V. K., IEEE Press (NY), USA, 1995.

23ECE210

MEMORY TECHNOLOGIES

(Program Elective - IV)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Digital System Design, VLSI Design.

COURSE OBJECTIVES: This course aims to
1. To acquire knowledge about different types of semiconductor memories.
2. To study about architecture and operations of different semiconductor memories.
3. To comprehend the low power design techniques and methodologies.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Summarize Static Random Access Memory Technologies.
2. Outline the concepts of dynamic random access memory technologies.
3. Demonstrate various nonvolatile memories.
4. Illustrate Memory Reliability and Radiation Effects.
5. Describe advanced memory technologies.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	1	3	2	1
CO 2	3	1	3	2	1
CO 3	3	1	3	1	1
CO 4	3	1	2	2	1
CO 5	3	2	3	1	1

UNIT – I

Random Access Memory Technologies: Static Random-Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT – II

DRAMs: MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs, SRAM and DRAM Memory Controllers.

UNIT – III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-Volatile SRAM, Flash Memories.

UNIT – IV

Advanced Memory Technologies And High-Density Memory Packing Technologies: Ferroelectric Random-Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random-Access Memories (MRAMs), Experimental Memory Devices.

UNIT – V

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

TEXT BOOKS:

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience.

2. Kiyoo Itoh, “VLSI memory chip design”, Springer International Ed.

SUGGESTED READING:

1. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability, PHI.
2. W. D. Brown, and Joe Brewer, Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices, Wiley-IEEE Press, 1997.

23ECE211

PHYSICAL DESIGN AUTOMATION

(Program Elective - IV)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Basic knowledge on Semiconductor Physics and MOS Transistors followed by Analog and Digital Fundamentals are required.

COURSE OBJECTIVES: This course aims to

1. Model passive and active devices suiting advances in IC fabrication technology.
2. Create learning, development and testing environment to meet ever challenging needs in the field of Chip Design.
3. Communicate effectively and convey ideas using innovative engineering using appropriate EDA tools.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Study automation process for VLSI system design.
2. Understand the fundamentals for VLSI system design.
3. Develop and enhance the existing computational techniques for physical design process of VLSI Circuits.
4. Study automation process for VLSI System design.
5. Understanding fundamentals for various physical design CAD tools.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	1	3	3	1
CO 2	3	1	3	3	1
CO 3	3	1	3	3	2
CO 4	3	1	2	3	1
CO 5	3	1	2	3	2

UNIT – I

Introduction To VLSI Systems: Introduction to IC Technology, Moore's Law, Design Representation, Hierarchical Abstraction, VLSI Design Styles, VLSI Design Flow, Different CMOS VLSI Design Fabrication Layers, VLSI Process Technology.

UNIT – II

Concepts of Physical Design and Design Rules: Introduction, Typical Structures of CMOS Fabrication Process-N-Well, P-Well and Twin Tub, CMOS Parasitic- Latch-Up and its Prevention. Cell Based Layout Design, Fabrication Errors, Interconnects, Contacts, Vias, SCMOS Design Rules, Lambda Based Design Rules, Stick Diagrams, Hierarchical Stick Diagrams, Layouts.

UNIT – III

Timing Analysis: Introduction, Delay in any VLSI Circuits, Design Techniques for Delay Reductions, Timing Models, Timing Analysis Goals, Timing Analysis at Chip Level, Static Timing Analysis, Checking Timing Constraints, Timing Verification in Sequential Circuits.

UNIT – IV

Physical Design: Introduction, Partitioning, Floor Planning, Placement, Routing, Block Placement, Global Routing, Switchbox Routing, Power Routing, Clock Routing, Floor Planning, Tips, Clock Distribution, Floor Planning, Special Routing, Multilevel Routing**,** Single Layer and Two-Layer Routing.

UNIT – V

EDA/CAD Tools: Parasitic Extraction, Design Rule Checkers, Layout versus Schematic Checkers, ERC, Layout Editors and Extractors, Circuit Extractors, Cross Talk Analysis, Electromigration, IR Drop, Physical Automations Of FPGAs.

TEXT BOOKS:

1. J.D.Plummer, M.D.Deal and P.B.Griffin, "The Silicon VLSI Technology Fundamentals", Practice and modeling, Pearson Education 2009.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", 2002.
3. Debaprasd Das, "VLSI design", Oxford University press, 2012.

SUGGESTED READING:

1. Modern VLSI Design (System on Chip), Woyne Wolf, Pearson Education, 2002.
2. S.H. Gerez, "Algorithms for VLSI Design Automation", 1998.

23ECE212

SoC DESIGN

(Program Elective - IV)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Concepts of ASIC, Digital Design, Microprocessors and Computer System Architecture.

COURSE OBJECTIVES: This course aims to

1. Classify the SoC design approaches using various variety of cores like RISC, CISC, NISC and ASIP and different interconnects.
2. Introduce architectural description languages for SoC Design.
3. Demonstrate various simulation and synthesis techniques available for SoC Design.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Utilize appropriate core from CISC, RISC, NISC, ASIP, etc. for the design of given SoC.
2. Able to judge and select appropriate ADL for the design exploration of SoC.
3. Choose appropriate interconnect for the SoC with proper justification.
4. Understand the importance of simulation and validation of the SoC.
5. Understand the process of synthesis of SoC.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	2	3	3	2
CO 2	3	2	3	3	2
CO 3	3	2	3	3	2
CO 4	1	2	2	3	2
CO 5	1	2	2	2	2

UNIT – I

Introduction To SoC: Architecture of Present Day SoCs, Design Issues Of SoC, Hardware Software Co-Design, Co-Design Flow, Co-Design Tools, EDA Tools for various Phases of SoC Design.

ASIC and NISC Overview: Overview of ASIC Types, CISC, RISC and NISC Approaches Application Specific Instruction Processor (ASIP) Concepts, NISC – NISC Control Words Methodology, NISC Applications and Advantages.

UNIT – II

ADL (for ASIP and NISC) and GNR: Introduction to Architecture Description Languages (ADLs), Classification of ADLs, Architecture Description Languages (ADL) for Design and Verification of Application Specific Instruction-Set Processors (ASIP)- Overview of NML, (NISC)-Design Flow, Modeling NISC Architectures and Systems, Generic Netlist representation - A Formal Language for Specification, Compilation and Synthesis of Embedded Processors.

UNIT – III

Low Power SoC Design: Low Power System Perspective - Power Gating, Clock Gating, Adaptive Voltage Scaling (AVS), Dynamic Clock Frequency and Voltage Scaling (DCFS), Power Consumption Verification.

Interconnects: Overview, Interconnect Architectures, Bus: Basic Architecture, Arbitration and Protocols, Bus Bridge, Physical Bus Structure, Bus Varieties, SoC Standard Buses: AMBA, Coreconnect, Bus Interface Units: Bus Sockets and Bus wrappers, Beyond the Bus: NOC with Switch Interconnects, Static Networks, Dynamic Networks, Some NOC Switch Examples.

UNIT – IV

Simulation, Validation & Testing: Different Simulation Modes: Behavioral, Functional, Gate Level, Transistor / Circuit Simulation, Static Timing Analysis, FPGA, Reconfigurable Systems. Design Validation, Core Level

Validation, Core Validation Plan, Test Benches, Core Level Timing Verification, Interface Verification, Gate Level Verification, SoC Design Validation, Co-Simulation, Emulation, SoC Test Issues, Core Test, Test Methodology for Design Reuse.

UNIT – V

Synthesis & Design: Clock Tree Synthesis, Technology Independent and Technology Dependent Approaches for Synthesis, Optimization Constraints, Synthesis Report Analysis. Case Study on ARM Based SoC Design.

TEXT BOOKS:

1. Michael J. Flynn and Wayne Luk, "Computer System Design: Systemon- Chip". Wiley, 2011.
2. RochitRajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000.

SUGGESTED READING:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006.
3. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008.

23ECE213

NANOMATERIALS AND NANOTECHNOLOGY

(Program Elective - V)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Basic knowledge in Nano-materials and Material Science.

COURSE OBJECTIVES: This course aims to

1. Describe the basic science behind the properties of materials at the Nanometer scale.
2. Understand the various micro and nano fabrication techniques.
3. Characterize Nano Structures and special Nano-materials.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Understand the basic electrical and optical, magnetic, mechanical properties of nano materials.
2. Construct devices based on nano-materials.
3. Explain nano fabrication steps, fabrication and applications of MEMS.
4. Construct Nano structures like Carbon nano tubes and MEM actuators.
5. Discuss various procedures of nano composites and applications of nano biomaterials.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	1	1	1	1	1
CO 2	2	1	1	1	1
CO 3	2	2	2	2	2
CO 4	2	2	3	2	3
CO 5	3	3	3	2	3

UNIT – I

Introduction to Nano-Materials: Evolution of Nano-Science and Technology, Introduction to Nanotechnology, Moore's Law, Bottom Up and Top – Down Approaches, Introduction to Semiconducting Nano Particles, Electrical and Optical Properties, Superconducting Properties, Magnetic Properties, Mechanical Properties.

UNIT – II

Applications Of Nano-Materials: Molecular Electronics and Nano-Electronics, NanoBOTs, Biological Applications of Nanoparticles, Catalysis by Gold Nano-Particles, Band Gap Engineered Quantum Devices-Quantum Well Devices, Quantum Dot Devices, Nano-Mechanics, Carbon Nanotube Emitters. Photo-Electro-Chemical Cells, Photonic Crystals and Plasmon Waveguides.

UNIT – III

Nano Fabrication: Introduction to Micro, Nano Fabrication, Lithography, Electron Beam Lithography, Thin Film Deposition. Nano and Micro-Electromechanical Systems (NMEMS), Types of MEMS, Fabrication of MEMS Assembling and Packaging, Applications of MEMS.

UNIT – IV

Nano Structures: Carbon Nanotubes and Nano Devices-Structural Design of Nano and MEMS Actuators and Sensors Configurations and Structural Design of Motion Nano and Micro- Structures.

UNIT – V

Special Nano-Materials: Nano Composites - Introduction, Synthesis Procedures, Various Systems (Metal Polymer and Metal Ceramics) Characterization Procedures, Applications, Nano Photonics Materials.
Nano Biomaterials: Introduction, Biocompatibility, Applications.

TEXT BOOKS:

1. Guozhongcao, “Nano Structures and Nano materials: Synthesis, properties and applications”, Imperial college press, 2004.
2. Lyschevski, Sergey Edward, “Nano and Microelectro Mechanical Systems”, Fundamentals of Nano and micro engineering, CRC Press, 2000.

SUGGESTED READING:

1. A.S Edelstein & R C Cammarata, “Nano Materials: Synthesis, Properties, and Applications”, Institute of physics publishing, 1996.

23ECE214

RECONFIGURABLE COMPUTING SYSTEMS

(Program Elective - V)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Knowledge of Digital Design using Multiplexers and Look-up tables.

COURSE OBJECTIVES: This course aims to
1. Study various Reconfigurable computing systems Architectures and its features.
2. Understand the different programming technologies, PAR, and testing.
3. Study the design flow and tools for FPGA and ASICs.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Describe the concepts of Reconfigurable computing systems and able to implement logic functions using them.
2. Analyze the various architectures of CPLD and FPGA.
3. Summarize the various features of advanced FPGAs.
4. Understand the concepts of placement and routing algorithms.
5. Demonstrate VLSI tool flow for FPGA and ASICs and relate the testing concepts.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	1	1	1	1
CO 2	3	1	1	1	1
CO 3	3	1	1	2	1
CO 4	2	1	1	1	1
CO 5	3	1	1	2	1

UNIT – I

Reconfigurable Computing Systems: Introduction, Evolution: Programmable Read only Memory (PROM), Programmable Logic Array (PLA) and Programmable Array Logic (PAL), Implementation with PLDs, Introduction to CPLD, FPGA and ASIC, Programming Technologies: SRAM, Anti Fuse, EEPROM and Flash Memory.

UNIT – II

CPLD: Complex Programmable Logic Devices: Architecture and Features of Altera Max 7000 Series CPLD, AMD Mach 4 and Xilinx 9500 Series.

FPGAs: Field Programmable Gate Arrays: Logic Blocks, Routing Architecture and Features of Xilinx XC4000, Spartan II, Virtex II and Actel Act1, Act2, Act3 FPGAs.

UNIT – III

Advance FPGAs: Architectures and Features of Xilinx Spartan- 6, Virtex-6, and Alteras Startix FPGAs. Introduction to Xilinx Zynq Board.

UNIT – IV

Placement: Objectives, Placement Algorithms: Min-Cut-Based Placement, Iterative Improvement Placement, Simulated Annealing. **Routing:** Objectives, Segmented Channel Routing, Maze Routing, Routability Estimation, Computing Signal Delay in RC Tree Networks.

UNIT – V

Design Flow and Testing: Design Flow for FPGA and ASIC, Digital Front End and Back-End Tools For FPGAs And ASICs, Verification: Introduction, Logic Simulation, Design Validation, Timing Verification, Testing

Concepts: Failures, Mechanisms and Faults, Fault Coverage, ATPG, BIST Methods and Programmability Failures.

TEXT BOOKS:

1. Hideharu Amano, "Principles and Structures of FPGAs" Springer Nature Singapore Pte Ltd. 2018
2. S. Brown, R. Francis, J. Rose, Z.Vransic, "Field Programmable Gate array", BSP, 2007.
3. P.K. Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Pearson Education 2009.

SUGGESTED READING:

1. S. Trimberger, Edr., "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.

23ECE215

UNIX & SCRIPTING LANGUAGES

(Program Elective - V)

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Network Theory, Analog Electronics, Analog CMOS VLSI Design.

COURSE OBJECTIVES: This course aims to
1. Introduce students the concept of Unix Operating systems.
2. Demonstrate the internal structure of Unix O.S.
3. Demonstrate Unix shell scripting.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Understand Unix operating system.
2. Analyze the organization of files and file system in UNIX.
3. Analyze and access UNIX files, processes, etc.
4. Develop simple Unix shell scripts.
5. Develop PERL scripts.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	2	3	3	3
CO 2	2	2	3	3	3
CO 3	2	2	3	3	3
CO 4	3	3	3	3	3
CO 5	3	3	3	3	3

UNIT – I

General Overview Of The System: System Structure, User Perspective, O/S Services Assumption about Hardware: The Kernel and Buffer Cache Architecture of Unix O/S, System Concepts, Kernel Data Structure, System Administration, Buffer Headers, Structure of the Buffer Pool, Scenarios for Retrieval of the Buffer, Reading and Writing Disk Block, Advantage and Disadvantage of Buffer Cache.

UNIT – II

Internal Representation of Files: INODES, Structure of Regular, Directories Conversions of a path name to an Inode, Super Block, Inode Assignment to a New File, Allocation of Disk Blocks, System Calls for the System: Open Read Write File and Record Close, File Creation, Operation of Special Files Change Directory and Change Root, Change Owner and Change Mode, STAT and FSTAT, PIPES Mounting and unmounting Files System, Link Unlink.

UNIT – III

Structures of Processes and Process Control: Process States and Transitions Layout of System Memory, the Context of a Process, Manipulation of Process Address Space, Sleep Process Creation / Termination, The User Id of a Process, Changing the Size of a Process. The SHELL Interprocess Communication and Multiprocessor System: Process Tracing System V IPO Network Communication Sockets Problem of Multiprocessors Systems, Solution with Master and Hare Process, and Solution with Semaphores.

UNIT – IV

Introduction to Shell Scripts: Shell Bourne Shell, C Shell, Unix Commands, Permissions, Editors, Filters, SED, GREP Family, Shell Variables, Scripts, Metacharacters and Environment, If and Case Statements, For, While and Until Loops. Shell Programming.

UNIT – V

Awk and Perl Programming: Awk Pattern Scanning and Processing Language, BEGIN and END Patterns, Awk Arithmetic and Variables, Awk Built in Variable Names and Operators, Arrays, Strings, Functions, Perl; The Chop() Function, Variable and Operators, $_ and $., Lists, Arrays, Regular Expression and Substitution, File Handling, Subroutines, Formatted Printing.

TEXT BOOKS:

1. M.J. Bach "Design of UNIX O.S. ", Prentice Hall of India.
2. Y.Kanetkar "Unix shell programming", BPB Pub.

SUGGESTED READING:

1. B.W. Kernighan & R. Pike, "The UNIX Programming Environment", Prentice Hall of India, 1995.

23MEM103

RESEARCH METHODOLOGY AND IPR

(Mandatory Course)

Instruction	2 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	2

PREREQUISITE: Fundamentals of Mathematical Analysis.

COURSE OBJECTIVES: This course aims to

1. Motivate to choose research as career
2. Formulate the research problem, prepare the research design
3. Identify various sources for literature review and data collection report writing
4. Equip with good methods to analyze the collected data
5. Know about IPR copyrights

COURSE OUTCOMES: After completion of this course, students will be able to

1. Define research problem, review and asses the quality of literature from various sources
2. Improve the style and format of writing a report for technical paper/ Journal report, understand and develop various research designs.
3. Collect the data by various methods: observation, interview, questionnaires.
4. Analyze problem by statistical techniques: ANOVA, F-test, and Chi-square.
5. Understand apply for patent and copyrights.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	2	1	2	2
CO 2	3	3	3	2	2
CO 3	3	2	2	1	2
CO 4	3	1	2	2	3
CO 5	3	3	3	3	3

UNIT - I

Research Methodology: Research Methodology: Objectives and Motivation of Research, Types of Research, research approaches, Significance of Research, Research Methods verses Methodology, Research Process, Criteria of Good Research, Problems Encountered by Researchers in India, Benefits to the society in general. Defining the Research Problem: Selection of Research Problem, Necessity of Defining the Problem

UNIT - II

Literature Survey Report writing: Literature Survey: Importance and purpose of Literature Survey, Sources of Information, Assessment of Quality of Journals and Articles, Information through Internet. Report writing: Meaning of interpretation, layout of research report, Types of reports, Mechanics of writing a report. Research Proposal Preparation: Writing a Research Proposal and Research Report, Writing Research Grant Proposal

UNIT - III

Research Design: Research Design: Meaning of Research Design, Need of Research Design, Feature of a Good Design, Important Concepts Related to Research Design, Different Research Designs, Basic Principles of Experimental Design, Developing a Research Plan, Steps in sample design, types of sample designs.

UNIT - IV

Data Collection and Analysis: Data Collection: Methods of data collection, importance of Parametric, non-parametric test, testing of variance of two normal population, use of Chi-square, ANOVA, Ftest, z-test

UNIT - V

Patents and Copyright: Patent: Macro economic impact of the patent system, Patent document, How to protectyour inventions. Granting of patent, Rights of a patent, how extensive is patent protection. Copyright: What is copyright. What is covered by copyright? How long does copyright last? Why protect copyright? Related Rights: what are related rights? Enforcement of Intellectual Property Rights: Infringement of intellectual property rights, Case studies of patents and IP Protection.

TEXT BOOKS:

1. C.R Kothari, "Research Methodology, Methods & Technique"; New Age International Publishers, 2004
2. R. Ganesan, "Research Methodology for Engineers", MJP Publishers , 2011
3. Y.P. Agarwal, "Statistical Methods: Concepts, Application and Computation", Sterling Publs., Pvt., Ltd., New Delhi, 2004.

SUGGESTED READING:

1. Ajit Parulekar and Sarita D' Souza, "Indian Patents Law – Legal & Business Implications"; Macmillan India ltd , 2006
2. B. L.Wadehra; "Law Relating to Patents, Trade Marks, Copyright, Designs & Geographical Indications"; Universal law Publishing Pvt. Ltd., India2000.
3. P. Narayanan; "Law of Copyright and Industrial Designs"; Eastern law House, Delhi 2010.

23CEA101

DISASTER MITIGATION AND MANAGEMENT

(Audit Course)

Instruction	2 L Hours per Week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	--
Credits	Non Credit

PREREQUISITE: Environmental science and general awareness about natural calamities.

COURSE OBJECTIVES: This course aims to

1. Equip the students with the basic knowledge of hazards, disasters, risks and vulnerabilities including natural, climatic and human induced factors and associated impacts.
2. Impart knowledge in students about the nature, causes, consequences and mitigation measures of the various natural disasters.
3. Enable the students to understand risks, vulnerabilities and human errors associated with human induced disasters.
4. Enable the students to understand and assimilate the impacts of any disaster on the affected area depending on its position/ location, environmental conditions, demographic, etc.
5. Equip the students with the knowledge of the chronological phases in a disaster management cycle and to create awareness about the disaster management framework and legislations in the context of national and global conventions.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Ability to analyse and critically examine existing programs in disaster management regarding vulnerability, risk and capacity at different levels.
2. Ability to understand and choose the appropriate activities and tools and set up priorities to build a coherent and adapted disaster management plan.
3. Ability to understand various mechanisms and consequences of human induced disasters for the participatory role of engineers in disaster management.
4. Understand the impact on various elements affected by the disaster and to suggest and apply appropriate measures for the same.
5. Develop an awareness of the chronological phases of disaster preparedness, response and relief operations for formulating effective disaster management plans and ability to understand various participatory approaches/strategies and their application in disaster management.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	3	2	1	1
CO 2	3	3	2	2	2
CO 3	2	3	3	2	2
CO 4	3	3	2	3	3
CO 5	3	2	2	3	3

UNIT – I

Introduction: Basic Definitions- Hazard, Disaster, Vulnerability, Risk, Resilience, Mitigation, Management; Classification of Types of Disaster - Natural and Man - Made; International Decade for Natural Disaster Reduction (IDNDR); International Strategy for Disaster Reduction (ISDR), National Disaster Management Authority (NDMA).

UNIT – II

Natural Disasters: Hydro meteorological disasters: Causes, Early warning systems- monitoring and management, structural and non-structural measures for floods, drought and Tropical cyclones; Geographical based disasters: Tsunami generation, causes, zoning, Early warning systems- monitoring and management, structural and non-structural mitigation measures for earthquakes, tsunami, landslides, avalanches and forest fires. Case studies related to various hydro meteorological and geographical based disasters.

UNIT – III

Human Induced Hazards: Chemical disaster- Causes, impacts and mitigation measures for chemical accidents, Risks and control measures in a chemical industry, chemical disaster management; Case studies related to various chemical industrial hazards eg: Bhopal gas tragedy; Management of chemical terrorism disasters and biological disasters; Radiological Emergencies and case studies; Case studies related to major power break downs, fire accidents, traffic accidents, oil spills and stampedes, disasters due to double cellar construction in multi-storied buildings.

UNIT – IV

Disaster Impacts: Disaster impacts- environmental, physical, social, ecological, economical, political, etc.; health, psycho-social issues; demographic aspects- gender, age, special needs; hazard locations; global and national disaster trends; climate change and urban disasters.

UNIT – V

Concept of Disaster Management: Disaster management cycle – its phases; prevention, mitigation, preparedness, relief and recovery; risk analysis, vulnerability and capacity assessment; Post-disaster environmental response- water, sanitation, food safety, waste management, disease control; Roles and responsibilities of government, community, local institutions, NGOs and other stakeholders; Policies and legislation for disaster risk reduction, DRR Programs in India and the activities of National Disaster Management Authority.

TEXT BOOKS:

1. Pradeep Sahni," Disaster Risk Reduction in South Asia", Prentice Hall, 2003.
2. B. K. Singh," Handbook of Disaster Management: techniques & Guidelines", Rajat Publication, 2008.

SUGGESTED READING:

1. Ministry of Home Affairs". Government of India, "National disaster management plan, Part I and II",
2. K. K. Ghosh," Disaster Management", APH Publishing Corporation, 2006.
3. Hazards, Disasters and your community: A booklet for students and the community, Ministry of home affairs.
4. http://www.indiaenvironmentportal.org.in/files/file/disaster_management_india1.pdf
5. http://www.ndmindia.nic.in/ (National Disaster management in India, Ministry of Home Affairs)

23EGA101

ENGLISH FOR RESEARCH PAPER WRITING

Instruction	2 L Hours per Week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	-
Credits	0

PREREQUISITE: Writing to express on science and technological concepts with good taste for research and development.

COURSE OBJECTIVES: This course aims to

1. Motivate learners for academic writing and thus encourage them for continuous professional updating and up-gradation.
2. Facilitate a practical understanding of the multiple purposes of Writing Research Papers and help them infer the benefits and limitations of research in science and technology.
3. Brainstorm and develop the content, formulating a structure and illustrating the format of writing a research paper.
4. Survey and select a theme/topic for a thorough reading and to writing a research paper.
5. Understand to implement the intricacies of writing and publishing a research paper.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Improve work performance and efficiency, illustrate the nuances of research paper writing and draw conclusions on professional usefulness.
2. Classify different types of research papers and organize the format and citation of sources.
3. Explore various formats of APA, MLA and IEEE and set up for writing a research paper.
4. Draft paragraphs and write theme based thesis statements in a scientific manner.
5. Develop an original research paper while acquiring the knowledge of how and where to publish their papers.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	2	2	1	2
CO 2	3	3	1	1	1
CO 3	3	3	2	1	1
CO 4	3	3	1	1	1
CO 5	3	3	2	1	1

UNIT - I

Academic Writing: Meaning & Definition of a research paper; Purpose of a research paper - Scope, Benefits, Limitations and outcomes for professional development, An introduction to methods and Approaches of Research.

UNIT - II

Research Paper Format: Title - Abstract - Introduction - Discussion - Findings - Conclusion - Style of Indentation - Font size/Font types - Indexing - Citation of sources.

UNIT - III

Process of Writing a Research Paper, Writing to Draft a Format, Develop Content, Adapting, Reviewing, Paraphrasing& Plagiarism Checks.

UNIT - IV

Choosing a topic - Thesis Statement - Outline - Organizing notes - Language of Research - Word order, Paragraphs - Writing first draft-Revising/Editing - The final draft and proof reading. Understanding APA, MLA, IEEE formats.

UNIT - V

Research Paper Publication Reputed Journals –Paid, Free and peer reviewed journals, National/International - ISSN No, No. of volumes, Scopus Index/UGC Journals. Getting Papers Published.

TEXT BOOKS:

1. Kothari, C. R. and Gaurav, Garg, "Research Methodology Methods and Techniques", 4thEdition, New Age International Publishers, New Delhi, 2019.
2. Ellison, Carroll. "Writing Research Papers", McGraw Hill's Concise Guide, 2010.
3. Lipson, Charles. "Cite Right: A Quick Guide to Citation Styles-- MLA, APA, Chicago, the Sciences, Professions, and More", 2nd Edition,. University of Chicago Press. Chicago, 2018.

SUGGESTED READING:

1. Day, Robert A. "How to Write and Publish a Scientific Paper", Cambridge University Press, 2006
2. Girden, E. R. "MLA Handbook for Writers of Research Papers", 7th Edition, East West Press Pvt. Ltd, New Delhi, 2009
3. Bailey, Stephen. "Academic Writing: A Handbook for International Students", Routledge, 2018

ONLINE RESOURCES:

1. https://onlin://onlinecourses.nptel.ac.in/noc 18_mg13/preview
2. https://nptel.ac.in/courses/121/106/121106007/
3. https://www.classcentral.com/course/swayam-introduction-to-research-5221

WRITING TOOLS:

1. https://owl.purdue.edu/owl_exercises/index.html - The Owl writing lab
2. https://www.turnitin.com/login_page.asp?lang=en_us – Turn tin software

23EGA102

CONSTITUTION OF INDIA

Instruction	2 L Hours per Week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	-
Credits	0

PREREQUISITE: Knowledge on basics of the Constitution and the Government.

COURSE OBJECTIVES: This course aims to

1. The history of Indian Constitution and its role in the Indian democracy.
2. Address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. Have knowledge of the various Organs of Governance and Local Administration.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Understand the making of the Indian Constitution and its features.
2. Understand the Rights of equality, the Right of freedom and the Right to constitutional remedies.
3. Have an insight into various Organs of Governance - composition and functions.
4. Understand powers and functions of Municipalities, Panchayats and Co-operative Societies.
5. Understand Electoral Process, special provisions.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	-	-	-	2
CO 2	2	-	-	-	2
CO 3	2	-	-	1	2
CO 4	2	-	-	1	2
CO 5	2	-	-	1	2

UNIT-I

History of making of the Indian constitutions - History, Drafting Committee (Composition & Working). **Philosophy of the Indian Constitution**: Preamble, Salient Features.

UNIT-II

Contours of Constitutional Rights and Duties - Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT-III

Organs of Governance - Parliament: Composition, Qualifications, Powers and Functions
Union executives : President, Governor, Council of Ministers, Judiciary, appointment and transfer of judges, qualifications, powers and functions.

UNIT-IV

Local Administration - District's Administration head: Role and importance. Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Panchayati Raj: Introduction, PRI: Zilla Panchayat, Elected Officials and their roles, CEO Zilla Panchayat: positions and role.
Block level: Organizational Hierarchy (Different departments) Village level: role of elected and appointed officials. Importance of grass root democracy.

UNIT-V

Election commission: Election Commission: Role and functioning, Chief Election Commissioner and Election Commissioners, State Election Commission: Role and functioning. Institute and Bodies for the welfare of SC/ST/OBC and women**.**

TEXT BOOKS:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Busi, S. N., Dr. B. R. Ambedkar, Framing of Indian Constitution'', 1st Edition, Ava Publishers, New Delhi, 2015.
3. Jain, M. P., "Indian Constitution Law", 7th Edition, Lexis Nexis, New Delhi, 2014.
4. Basu, D.D. "Introduction to the Constitution of India", Lexis Nexis, New Delhi. 2015.

SUGGESTED READING:

1. Bhargava, Rajeev. (ed), "Politics and Ethics of the Indian Constitution", OUP, 2008.
2. NCERT, Indian Constitution at Work, 1st Edition, Government of India, New Delhi 2006, reprinted in 2022.
3. Ravindra Sastry, V. (ed.), Indian Government & Politics, 2nd edition, Telugu Akademy, 2018.

ONLINE RESOURCES:

1. http://www.nptel.ac.in/courses/103107084/Script.pdf

23ADA101

PEDAGOGY STUDIES

(Audit Course)

Instruction	2 L Hours per Week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	--
Credits	Non Credit

PREREQUISITE: Teacher education, Curriculum and Assessment.

COURSE OBJECTIVES: This course aims to

1. Present the basic concepts of design and policies of pedagogy studies.
2. Provide understanding of the abilities and dispositions with regard to teaching techniques, curriculum design and assessment practices.
3. Familiarize various theories of learning and their connection to teaching practice.
4. Create awareness about the practices followed by DFID, other agencies and other researchers.
5. Provide understanding of critical evidence gaps that guides the professional development

COURSE OUTCOMES: After completion of this course, students will be able to

1. Illustrate the pedagogical practices followed by teachers in developing countries both in formal and informal classrooms.
2. Examine the effectiveness of pedagogical practices.
3. Understand the concept, characteristics and types of educational research and perspectives of research.
4. Describe the role of classroom practices, curriculum and barriers to learning.
5. Understand Research gaps and learn the future directions

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	1	1	1	2	2
CO 2	1	1	1	2	2
CO 3	2	2	2	2	2
CO 4	1	1	1	2	2
CO 5	2	2	2	2	2

UNIT – I

Introduction and Methodology: Aims and Rationale, Policy Background, Conceptual Framework and Terminology – Theories of Learning, Curriculum, Teacher Education - Conceptual Framework, Research Questions – Overview of Methodology and Searching.

UNIT – II

Thematic Overview: Pedagogical Practices followed by Teachers in Formal and Informal Classrooms in Developing Countries – Curriculum, Teacher Education.

UNIT – III

Evidence on the Effectiveness of Pedagogical Practices: Methodology for the in Depth Stage: Quality Assessment of Included Studies - How can Teacher Education (Curriculum And Practicum) and the School Curriculum and Guidance Material Best Support Effective Pedagogy? - Theory of Change - Strength and Nature of the Body of Evidence for Effective Pedagogical Practices - Pedagogic Theory and Pedagogical Approaches - Teachers' Attitudes and Beliefs and Pedagogic Strategies.

UNIT – IV

Professional Development: Alignment with Classroom Practices and Follow up Support - Support from the Head Teacher and the Community – Curriculum and Assessment - Barriers to Learning: Limited Resources and Large Class Sizes.

UNIT – V

Research Gaps and Future Directions: Research Design – Contexts – Pedagogy - Teacher Education - Curriculum and Assessment – Dissemination and Research Impact.

TEXT BOOKS:

1. Ackers J, Hardman F, "Classroom Interaction in Kenyan Primary Schools, Compare", 31 (2): 245 – 261, 2001.
2. Agarwal M, "Curricular Reform in Schools: The importance of evaluation", Journal of Curriculum Studies, 36 (3): 361 – 379, 2004.

SUGGESTED READING:

1. Akyeampong K, "Teacher Training in Ghana – does it count? Multisite teacher education research project (MUSTER)", Country Report 1.London: DFID, 2003.
2. Akyeampong K, Lussier K, Pryor J, Westbrook J, "Improving teaching and learning of Basic Maths and Reading in Africa: Does teacher Preparation count? International Journal Educational Development, 33 (3): 272- 282, 2013.
3. Alexander R J, "Culture and Pedagogy: International Comparisons in Primary Education", Oxford and Boston: Blackwell, 2001.
4. Chavan M, "Read India: A mass scale, rapid, 'learning to read' campaign", 2003.

WEB RESOURCES:

1. https://onlinecourses.nptel.ac.in/noc17_ge03/preview.
2. www.pratham.org/images/resources%20working%20paper%202.pdf.

23EGA104

PERSONALITY DEVELOPMENT THROUGH LIFE'S ENLIGHTENMENT SKILLS

Instruction	2 L Hours per Week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	-
Credits	0

PREREQUISITE: Awareness on Personality Development.

COURSE OBJECTIVES: This course aims to

1. Learn to achieve the highest goal happily.
2. Become a person with stable mind, pleasing personality and determination.
3. Awake wisdom among themselves.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Develop their personality and achieve their highest goal of life.
2. Lead the nation and mankind to peace and prosperity.
3. Practice emotional self-regulation.
4. Develop a positive approach to work and duties.
5. Develop a versatile personality.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	1	-	-	2
CO 2	2	1	-	-	2
CO 3	2	1	-	-	2
CO 4	2	1	-	-	2
CO 5	2	1	-	-	2

UNIT - I

Neetisatakam – Holistic development of personality - Verses 19, 20, 21, 22 (Wisdom) - Verses 29, 31, 32 (Pride and Heroism) - Verses 26,28,63,65 (Virtue).

UNIT – II

Neetisatakam – Holistic development of personality (cont'd) - Verses 52, 53, 59 (dont's) - Verses 71, 73, 75 & 78 (do's) - Approach to day to day works and duties.

UNIT - III

Introduction to Bhagavadgeetha for Personality Development – Shrimad Bhagawad Geeta: Chapter 2– Verses 41, 47, 48 - Chapter 3 – Verses 13,21,27,35 - Chapter 6 – Verses 5,13,17,23,35 - Chapter 18 – Verses 45, 46, 48 Chapter – 6: Verses 5, 13, 17, 23, 35; Chapter – 18: Verses 45, 46, 48.

UNIT - IV

Statements of basic knowledge – Shrimad Bhagawad Geeta: Chapter 2- Verses 56, 62, 68 - Chapter 12 – Verses 13, 14, 15, 16, 17, 18 - Personality of Role model from Shrimad Bhagawat Geeta.

UNIT - V

Role of Bahgavadgeeta in the present scenario - Chapter 2 – Verses 17 - Chapter 3 – Verses 36, 37, 42 - Chapter 4 – Verses 18, 38, 39 - Chapter 18 – Verses 37, 38, 63.

TEXT BOOKS:

1. Gopinath, P., "Bhartrihari's Three Satakam(Niti-sringar-vairagya)", Rashtriya Sanskrit Sansthanam, New Delhi, 2018.
2. Swarupananda, Swami, "Srimad Bhagavad Geeta", Advaita Ashram (Publication Dept), Kolkata, 2017.

ONLINE RESOURCES:

1. http://nptel.ac.in/downloads/109104115/

23EEA101

SANSKRIT FOR TECHNICAL KNOWLEDGE

(Audit Course)

Instruction	2 L Hours per Week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	--
Credits	Non Credit

PREREQUISITE: Basic knowledge in Samskrutham.

COURSE OBJECTIVES: This course aims to

1. Get a working knowledge in illustrious Sanskrit, the scientific language in the world.
2. Make the novice Learn the Sanskrit to develop the logic in mathematics, science & other subjects.
3. Explore the huge knowledge from ancient Indian literature.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Develop passion towards Sanskrit language.
2. Decipher the latent engineering principles from Sanskrit literature.
3. Correlates the technological concepts with the ancient Sanskrit history.
4. Develop knowledge for the technological progress.
5. Explore the avenue for research in engineering with aid of Sanskrit.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	1	1	1	1	1
CO 2	2	1	1	1	1
CO 3	2	1	1	1	1
CO 4	2	1	1	1	1
CO 5	1	1	1	1	1

UNIT –I

Introduction To Sanskrit Language: Sanskrit Alphabets – Vowels – Consonants – Significance of Amarakosa –Parts of Speech – Morphology – Creation of New Words – Significance of Synonyms – Sandhi – Samasa – Sutras –Active and Passive Voice – Past / Present / Future Tense – Syntax – Simple Sentences (Elementary Treatment Only).

UNIT – II

Role of Sanskrit in Basic Sciences: Brahmagupthas Lemmas (Second Degree Indeterminate Equations), Sum of Squares of N – Terms of AP – Sulba Sutram or Baudhayana Theorem (Origination of Pythogorous Theorem) – Value of Pie - Madhava's Sine and Cosine Theory (Origination of Taylor's Series). The Measurement System – Time – Mass – Length – Temp, Matter Elasticity – Optics – Speed of Light (Origination of Michealson and Morley Theory).

UNIT – III

Role of Sanskrit in Engineering – I (Civil, Mechanical, Electrical and Electronics Engineering): Building Construction – Soil Testing – Mortar – Town Planning – Machine Definition – Crucible – Furnace – Air Blower – Generation of Electricity in a Cell – Magnetism – Solar System – Sun: The Source of Energy, The Earth – Pingala Chandasutram (Origination of Digital Logic System).

UNIT – IV

Role of Sanskrit in Engineering – II (Computer Science Engineering & Information Technology): Computer Languages and the Sanskrit Languages - Computer Command Words and the Vedic Command Words – Analogy of Pramana in Memamsa with Operators in Computer Language – Sanskrit Analogy of Physical Sequence and Logical Sequence, Programming.

UNIT – V

Role of Sanskrit in Engineering – III (Bio-Technology and Chemical Engineering): Classification of Plants – Plants, The Living – Plants have Senses – Classification of Living Creatures. Chemical Laboratory Location and Layout – Equipment – Distillation Vessel – Kosthi Yanthram.

TEXT BOOKS:

1. M Krishnamachariar, "History of Classical Sanskrit Literature", TTD Press, 1937.
2. Kpail Kapoor, Language, "Linguistics and Literature: The Indian Perspective", ISBN-10: 8171880649, 1994.
3. "Pride of India", Samskrita Bharti Publisher, ISBN: 81-87276-27-4, 2007
4. Shri Rama Verma, "Vedas the source of ultimate science", Nag publishers, ISBN: 81-7081-618-1, 2005.

SUGGESTED READING:

1. "The Wonder that is Sanskrit", AuroPublications, ISBN: 978-8170601821, 2017.
2. "Science in Sanskrit", Samskrita Bharti Publisher, ISBN-13: 978-8187276333, 2007.

23EGA103

STRESS MANAGEMENT BY YOGA

Instruction	2 L Hours per Week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	-
Credits	0

PREREQUISITE: Knowledge on Yoga Practices.

COURSE OBJECTIVES: This course aims to
1. Create awareness about different types of stress and the role of yoga in the management of stress.
2. Promote positive health and overall well-being (Physical, mental, emotional, social and spiritual).
3. Prevent stress related health problems by yoga practice.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Understand yoga and its benefits.
2. Enhance Physical strength and flexibility.
3. Learn to relax and focus.
4. Relieve physical and mental tension through asanas.
5. Improve work performance and efficiency.

CO-PO ARTICULATION MATRIX

PO/PSO CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	1	-	-	2
CO 2	2	1	-	-	2
CO 3	2	1	-	-	2
CO 4	2	1	-	-	2
CO 5	2	1	-	-	2

UNIT - I

Meaning and definition of Yoga - Historical perspective of Yoga - Principles of Astanga Yoga by Patanjali).

UNIT - II

Meaning and definition of Stress - Types of stress - Eustress and Distress. Anticipatory Anxiety and Intense Anxiety and depression. Meaning of Management- Stress Management.

UNIT - III

Concept of Stress according to Yoga - Stress assessment methods - Role of Asana, Pranayama and Meditation in the management of stress.

UNIT - IV

Asanas- (5 Asanas in each posture) - Warm up - Standing Asanas - Sitting Asanas - Prone Asanas - Supine asanas - Surya Namaskar.

UNIT – V

Pranayama- Anulom and Vilom Pranayama - Nadishudhi Pranayama - Kapalabhati Pranayama - Bhramari Pranayama - Nadanusandhana Pranayama.

Meditation techniques: Om Meditation - Cyclic meditation: Instant Relaxation technique (QRT), Quick Relaxation Technique (QRT), Deep Relaxation Technique (DRT)

TEXT BOOKS:

1. Janardhan, Swami, "Yogic Asanas for Group Training - Part-I": Yogabhyasi Mandal, Nagpur.
2. Vivikananda, Swami**.** "Rajayoga or Conquering the Internal Nature", Advaita Ashrama (Publication Department), Kolkata.
3. Nagendra H.R and R. Nagaratna, “Yoga Perspective in Stress Management”, Swami Vivekananda Yoga Prakashan, Bangalore.

ONLINE RESOURCES:

1. https://onlinecourses.nptel.ac.in/noc16_ge04/preview
2. https://freevideolectures.com/course/3539/indian-philosophy/11

23ECA101

VALUE EDUCATION

(Audit Course)

Instruction	2 L Hours per Week
Duration of SEE	2 Hours
SEE	50 Marks
CIE	--
Credits	Non-Credit

PREREQUISITE: Knowledge about Universal Human values.

COURSE OBJECTIVES: This course aims to
1. Understand Value Education, Self-development and National development.
2. Imbibe good human values and Morals in students.
3. Cultivate individual and National character.

COURSE OUTCOMES: After completion of the Course, Students will be able to:
1. Summarize classification of values and values for self-development.
2. Identify the importance of values in personal and professional life.
3. Apply the importance of social values for better career and relationships.
4. Compile the values from holy books for personal and social responsibility.
5. Discuss concept of soul and reincarnation, values Dharma, Karma and Guna.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	2	2	2	2	3
CO 2	2	2	2	2	3
CO 3	2	2	2	2	3
CO 4	2	2	2	2	3
CO 5	2	2	2	2	3

UNIT – I

Human Values, Ethics and Morals: Concept of Values, Human Values, Indian Concept of Humanism, Values for Self-Development, Social Values, Individual Attitudes, Work Ethics, Moral and Non – Moral Behavior, Standards and Principles based on Religion, Culture and Tradition.

UNIT –II

Value Cultivation and Self-Management: Need and Importance of Cultivation of Values such as Sense – of Duty, Devotion to Work, Self – Reliance, Confidence, Concentration, Integrity & Discipline and Truthfulness.

UNIT – III

Spiritual Outlook and Social Values: Personality and Behavior Development, Scientific Attitude and Spiritual (Soul) Outlook, Cultivation of Social Values such as Positive Thinking, Punctuality, Love & Kindness, Avoiding Fault finding in others, Reduction of Anger, Forgiveness, Dignity of Labor, True Friendship, Universal Brotherhood and Religious Tolerance., Happiness vs Suffering, Love for Truth, Aware of Self – Destructive Habits, Appreciation and Co-Operation.

UNIT – IV

Values in Holy Books: Self – Management, Good Health and Internal & External Cleanliness**,** Holy Books versus Blind Faith, Character and Competence, Equality, Nonviolence, Humility, Role of Women.

UNIT – V

All Religions and Same Message: Mind your Mind, Self – Control**,** Concept of Soul, Science of Reincarnation, Character and Conduct, Concept of Dharma, Cause and Effect based Karma Theory, The Qualities of Devine and Devilish, Satwic, Rajasic and Tamasic Gunas.

TEXT BOOKS:

1. Chakroborty, S.K. “Values & Ethics for organizations Theory and practice”, Oxford University Press, New Delhi, 1998.
2. Jaya Dayal Goyandaka, “Srimad Bhagavad Gita”, with Sanskrit Text, Word meaning and Prose meaning, Gita Press, Gorakhpur, 2017.

SUGGESTED READING:

1. R R Gaur, R Asthana, G P Bagaria, “A Foundation Course in Human Values and Professional Ethics”, 2nd Revised Edition, Excel Books, New Delhi, 2019. ISBN 978-93-87034-47-1 The teacher’s manual

23CSO101

BUSINESS ANALYTICS

Open Elective – VI

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PRE-REQUISITES: Basic of programming, basic mathematics**.**

COURSE OBJECTIVES: This course aims to

1. Understanding the basic concepts of business analytics and applications.
2. Study various business analytics methods including predictive, prescriptive and prescriptive analytics.
3. Prepare the students to model business data using various data mining, decision making methods.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Identify and describe complex business problems in terms of analytical models.
2. Apply appropriate analytical methods to find solutions to business problems that achieve stated objectives.
3. Interpret various metrics, measures used in business analytics
4. Illustrate various descriptive, predictive and prescriptive methods and techniques.
5. Model the business data using various business analytical methods and techniques.
6. Create viable solutions to decision making problems.

CO-PO ARTICULATION MATRIX

CO/PO	PO1	PO2	PO3	PO4	PEO1	PEO2	PEO3
CO1	3	2	2	1	1	-	-
CO2	3	3	2	1	-	3	3
CO3	3	3	3	1	-	-	-
CO4	3	3	3	1	-	-	-
CO5	3	3	3	1	-	-	-
CO6	3	3	3	1	-	-	-

UNIT - I

Introduction to Business Analytics: Introduction to Business Analytics, need and science of data driven (DD) decision making, Descriptive, predictive, prescriptive analytics and techniques, Big data analytics, Web and Social media analytics, Machine Learning algorithms, framework for decision making, challenges in DD decision making and future.

UNIT - II

Descriptive Analytics: Introduction, data types and scales, types of measurement scales, population and samples, measures of central tendency, percentile, decile and quadrille, measures of variation, measures of shape-skewness, data visualization.

UNIT - III

Forecasting Techniques: Introduction, time-series data and components, forecasting accuracy, moving average method, single exponential smoothing, Holt's method, Holt-Winter model, Croston's forecasting method, regression model for forecasting, Auto regression models, auto-regressive moving process, ARIMA, Theil's coefficient

UNIT - IV

Decision Trees: CHAID, Classification and Regression tree, splitting criteria, Ensemble and method and randomforest. Clustering: Distance and similarity measures used in clustering, Clustering algorithms, K-Means and Hierarchical algorithms, Prescriptive Analytics- Linear Programming (LP) and LP model building,

UNIT-V

Six Sigma: Introduction, introduction, origin, 3-Sigma Vs Six-Sigma process,cost of poor quality, sigma score, industry applications, six sigma measures, DPMO, yield, sigma score, DMAIC methodology, Six Sigma toolbox.

TEXTBOOKS:

1. U Dinesh Kumar, "Business Analytics", Wiley Publications, 1st Edition, 2017
2. Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, "Business analytics Principles, Concepts, and Applications with SAS", Associate Publishers, 2015

SUGGESTED READINGS:

1. S. Christian Albright, Wayne L. Winston, "Business Analytics - Data Analysis and Decision Making",5th Edition, Cengage, 2015.

23MEO103

COMPOSITE MATERIALS

(Open Elective)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Basic knowledge of Engineering Materials and Mechanics.

COURSE OBJECTIVES: This course aims to
1. Composite materials and their constituents.
2. Classification of the reinforcements and evaluate the behaviour of composites.
3. Fabrication methods of metal matrix composites.
4. Manufacturing of Polymer matrix composites.
5. Failure mechanisms in composite materials.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Classify and characterize the composite materials.
2. Describe types of reinforcements and their properties.
3. Understand different fabrication methods of metal matrix composites.
4. Understand different fabrication methods of polymer matrix composites.
5. Decide the failure of composite materials.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	1	3	1	1
CO 2	3	1	3	1	1
CO 3	3	2	3	1	1
CO 4	3	2	3	1	1
CO 5	3	1	3	1	1

UNIT – I

Introduction: Definition – Classification and Characteristics of Composite Materials. Advantages and Application of Composites. Functional Requirements of Reinforcement and Matrix. Effect of Reinforcement (Size, Shape, Distribution, Volume Fraction) on Overall Composite Performance.

UNIT – II

Reinforcements: Preparation – Layup, Curing, Properties and Applications of Glass Fibers, Carbon Fibers, Kevlar Fibers and Boron Fibers. Properties and Applications of Whiskers, Particle Reinforcements. Mechanical Behavior of Composites: Rule of Mixtures, Inverse Rule of Mixtures. Isostrain and Isostress Conditions.

UNIT – II

Manufacturing of Metal Matrix Composites: Casting – Solid State Diffusion Technique, Cladding – Hot Isostatic Pressing. Properties and Applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid Phase Sintering. Manufacturing of Carbon – Carbon Composites: Knitting, Braiding, Weaving. Properties and Applications.

UNIT – IV

Manufacturing of Polymer Matrix Composites: Preparation of Moulding Compounds and Prepegs – Hand Layup Method – Autoclave Method – Filament Winding Method – Compression Moulding – Reaction Injection Moulding. Properties and Applications.

UNIT – V

Strength: Lamina Failure Criteria - Strength Ratio, Maximum Stress Criteria, Maximum Strain Criteria, Interacting Failure Criteria, Hygrothermal Failure. Laminate First Play Failure - Insight Strength.

TEXT BOOKS:

1. K.K.Chawla, "Composite Materials- Science and Engineering", 4th edition, Springer Verlag, 2019.
2. WD Callister, Jr., Adapted by R. Balasubramaniam , "Materials Science and Engineering, An introduction"., John Wiley & Sons, NY, Indian edition, 2007.

SUGGESTED READING:

1. Deborah D.L. Chung, "Composite Materials Science and Applications" 2nd edition, Springer Verlag, 2010.
2. Sanjay K. Mazumdar, "Composites Manufacturing- materials, product and process engineering", 1st edition, CRC press, 2002.
3. Daniel Gay, "Composite Materials Design and Applications" 3rd edition, CRC press, 2015.

23CEO101

COST MANAGEMENT OF ENGINEERING PROJECTS

(Open Elective)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Basics of Planning and Management**.**

COURSE OBJECTIVES: This course aims to

1. To enable students to understand the concepts of project management, project planning, and scheduling.
2. To provide knowledge of project monitoring and cost management.
3. To understand the concepts of budgetary control and Quantitative techniques for cost management.

COURSE OUTCOMES: After completion of this course, students will be able to

1. Acquire in-depth knowledge about the concepts of project management and understand the principles of project management.
2. Determine the critical path of a typical project using CPM and PERT techniques.
3. Prepare a work break down plan and perform linear scheduling using various methods.
4. Solve problems of resource scheduling and levelling using network diagrams.
5. Learn the concepts of budgetary control and apply quantitative techniques for optimizing project cost.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	1	2	1	2	1
CO 2	1	2	1	1	1
CO 3	3	2	2	1	1
CO 4	3	2	2	1	1
CO 5	1	1	1	1	1

UNIT - I

Project Management: Introduction to project managements, stakeholders, roles, responsibilities and functional relationships. Principles of project management, objectives and project management system. Project team, organization, roles, and responsibilities. Concepts of project planning, monitoring, staffing, scheduling and controlling.

UNIT - II

Project Planning and Scheduling: Introduction for project planning, defining activities and their interdependency, time and resource estimation. Work break down structure. Linear scheduling methods-bar charts, line of balance (lob), their limitations. Principles, definitions of network-based scheduling methods: CPM, PERT. Network representation, network analysis-forward and backward passes.

UNIT - III

Project Monitoring and Cost Analysis: Introduction-cost concepts in decision- making; relevant cost, differential cost, incremental cost and opportunity cost. objectives of a costing system; inventory valuation; creation of a database for operational control; provision of data for decision-making, time cost tradeoff- crashing project schedules, its impact on time on time, cost. Project direct and indirect costs.

UNIT - IV

Resources Management and Costing-Variance Analysis: Planning, enterprise resource planning, resource scheduling and levelling. Total quality management and theory of constraints. Activity-based cost management, bench marking; balanced score card and value-chain analysis

Standard Costing and Variance Analysis. Pricing strategies: praetor analysis. Target costing, life cycle costing. Costing of service sector. Just-in-time approach, material requirement

UNIT - V

Budgetary Control: Flexible budgets; performance budgets; zero-based budgets. Measurement of divisional profitability pricing decisions including transfer pricing.

Quantitative techniques for cost management: Linear programming, PERT/CPM, transportation assignment problems, simulation, learning curve theory.

TEXT BOOKS:

1. Charles T Horngren "Cost Accounting A Managerial Emphasis", Pearson Education; 14th edition 2012.
2. Charles T. Horngren and George Foster, "Advanced Management Accounting" Prentice-Hall; 6th Revised edition, 1987.
3. Robert S Kaplan Anthony A. Atkinson, "Management & Cost Accounting", Pearson; 2nd edition, 1996.
4. K. K Chitkara, "Construction Project Management: Planning, scheduling and controlling", Tata McGraw-Hill Education. 2004.
5. Kumar Neeraj Jha "Construction Project Management Theory and Practice", Pearson Education India; 2nd edition, 2015.

23MEO101

INDUSTRIAL SAFETY

(Open Elective)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Awareness about Mechanical and Electrical hazards.

COURSE OBJECTIVES: This course aims to

1. Familiarize causes for industrial accidents and preventive steps to be taken.
2. Elucidate fundamental concepts of Maintenance Engineering.
3. Explain about wear and corrosion along with preventive steps to be taken
4. Provide basic concepts and importance of fault tracing.
5. Provide steps involved in carrying out periodic and preventive maintenance of various equipment used in industry

COURSE OUTCOMES: After completion of this course, students will be able to

1. Identify the causes for industrial accidents and suggest preventive measures.
2. Identify the basic tools and requirements of different maintenance procedures.
3. Apply different techniques to reduce and prevent Wear and corrosion in Industry.
4. Identify different types of faults present in various equipments like machine tools, IC Engines, boilers etc.
5. Apply periodic and preventive maintenance techniques as required for industrial equipment like motors, pumps and air compressors and machine tools etc.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	3	3	3	2
CO 2	3	3	3	2	2
CO 3	3	1	3	2	1
CO 4	3	1	3	2	1
CO 5	3	2	3	3	3

UNIT - I

Industrial Safety: Accident, Causes, Types, Results and control, Mechanical and electrical hazards, Types, Causes and preventive steps/procedure, Describe salient points of factories act 1948 for health and safety, Wash rooms, Drinking water layouts, Light, Cleanliness, Fire, Guarding, Pressure vessels, Safety color codes, Fire prevention and firefighting, Equipment and methods.

UNIT - II

Fundamentals of Maintenance Engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT - III

Wear and Corrosion and their Prevention: Wear, Types, Causes, Effects, Wear reduction methods, Lubricants, Types and applications, Lubrication methods, General sketch, Working and applications of Screw down grease cup, Pressure grease gun, Splash lubrication, Gravity lubrication, Wick feed lubrication, Side feed lubrication, Ring lubrication, Definition of corrosion, principle and factors affecting the corrosion, Types of corrosion, Corrosion prevention methods.

UNIT - IV

Fault Tracing: Fault tracing, Concept and importance, Decision tree concept, Need and applications, Sequence of fault finding activities, Show as decision tree, Draw decision tree for problems in machine tools, Hydraulic,

Pneumatic, Automotive, Thermal and electrical equipment's like any one machine tool, Pump, Air compressor, Internal combustion engine, Boiler, Electrical motors, Types of faults in machine tools and their general causes.

UNIT - V

Periodic and Preventive Maintenance: Periodic inspection, Concept and need, Degreasing, Cleaning and repairing schemes, Overhauling of mechanical components, Overhauling of electrical motor, Common troubles and remedies of electric motor, Repair complexities and its use, Definition, Need, Steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of Machine tools, Pumps, Air compressors, Diesel generating sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, Advantages of preventive maintenance, Repair cycle concept and importance

TEXT BOOKS:

1. H. P. Garg, "Maintenance Engineering", S. Chand and Company.
2. Audels, "Pump-hydraulic Compressors", Mcgraw Hill Publication.

SUGGESTED READING:

1. Higgins & Morrow, "Maintenance Engineering Handbook", Da Information Services.
2. Winterkorn, Hans, "Foundation Engineering Handbook", Chapman & Hall London.

23MEO102

INTRODUCTION TO OPTIMIZATION TECHNIQUES

(Open Elective)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Basic knowledge of Mathematics.

COURSE OBJECTIVES: This course aims to
1. Come to know the formulation of LPP models.
2. Understand the Transportation and Assignment techniques.
3. Come to know the procedure of Project Management along with CPM and PERT techniques.
4. Understand the concepts of queuing theory and inventory models.
5. Understand sequencing techniques.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Formulate a linear programming problems (LPP).
2. Build and solve Transportation Models and Assignment Models.
3. Apply project management techniques like CPM and PERT to plan and execute project successfully.
4. Apply queing and inventory concepts in industrial applications.
5. Apply sequencing models in industries.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	3	1	3	1	2
CO 2	3	1	3	1	2
CO 3	1	1	3	2	3
CO 4	2	1	3	2	2
CO 5	2	1	3	3	2

UNIT – I

Operations Research: Definition, Scope, Models, Linear Programming Problems (LPP), Formulation, Graphical Method and Simplex Method.

UNIT – II

Transportation Models: Finding an Initial Feasible Solution - North West Corner Method, Least Cost Method, Vogel's Approximation Method, Finding the Optimal Solution, Special Cases in Transportation Problems - Unbalanced Transportation Problem, Degeneracy in Transportation, Profit Maximization in Transportation.

UNIT – III

Project Management: Definition, Procedure and Objectives of Project Management, Differences between PERT and CPM, Rules for Drawing Network Diagram, Scheduling the Activities, Fulkerson's Rule, Earliest and Latest Times, Determination of ES and EF Times in Forward Path, LS & LF Times in Backward Path, Determination of Critical Path, Duration of the Project, Free Float, Independent Float and Total Float.

UNIT – IV

Queuing Theory And Inventory: Kendols Notation, Single Server Models, Inventory Control - Deterministic Inventory Models - Probabilistic Inventory Control Models.

UNIT – V

Sequencing Models: Introduction, Objectives, General Assumptions, Processing 'N' Jobs through Two Machines, Processing 'N' Jobs Through Three Machines.

TEXT BOOKS:

1. H.A. Taha, “Operations Research, An Introduction”, PHI, 2008.
2. H.M. Wagner, “Principles of Operations Research”, PHI, Delhi, 1982.
3. J.C. Pant, “Introduction to Optimisation: Operations Research”, Jain Brothers, Delhi, 2008.

SUGGESTED READING:

1. Hitler Libermann, “Operations Research”, McGraw Hill Pub.2009.
2. Harvey M Wagner, “Principles of Operations Research”, Prentice Hall of India, 2010.

23EEO101

WASTE TO ENERGY

(Open Elective)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	60 Marks
CIE	40 Marks
Credits	3

PREREQUISITE: Prior knowledge of Energy Conversions.

COURSE OBJECTIVES: This course aims to
1. Know the various forms of waste
2. The extraction of Energy from Waste.
3. Infer the Global and national scenario.

COURSE OUTCOMES: After completion of this course, students will be able to
1. Understand the concept of waste to energy.
2. Explore the various Energy extraction options.
3. Describe the Energy Production methodology.
4. Explicate the Environmental implications.
5. Compare and contrast waste to energy productions by case studies.

CO-PO ARTICULATION MATRIX

PO/CO	PO1	PO2	PO3	PO4	PO5
CO 1	1	1	1	1	1
CO 2	2	1	1	1	2
CO 3	2	1	1	1	2
CO 4	1	1	1	1	1
CO 5	2	2	1	1	2

UNIT - I

Introduction: The Principles of Waste Management and Waste Utilization. Waste Management Hierarchy and 3R Principle of Reduce, Reuse and Recycle. Waste as a Resource and Alternate Energy source. Waste Sources & Characterization Waste production in different sectors such as domestic, industrial, agriculture, postconsumer, waste etc. Classification of waste – agro based, forest residues, domestic waste, industrial waste (hazardous and non-hazardous). Characterization of waste for energy utilization. Waste Selection criteria.

UNIT - II

Energy Extraction Options: Landfill gas, collection and recovery. Refuse Derived Fuel (RDF) – fluff, briquettes, pellets. Alternate Fuel Resource (AFR) – production and use in Cement plants, Thermal power plants and Industrial boilers. Conversion of wastes to fuel resources for other useful energy applications Energy from Plastic Wastes: Non-recyclable plastic wastes for energy recovery. Energy Recovery from waste and optimization of its use, benchmarking and standardization. Energy Analysis

UNIT - III

Energy production Methodologies: Collection, segregation, transportation and storage requirements. Location and Siting of 'Waste to Energy' plants. Industry Specific Applications: In-house use: sugar, distillery, pharmaceuticals, Pulp and paper, refinery and petrochemical industry and any other industry. Centralized and Decentralized Energy production, distribution and use. Comparison of Centralized and decentralized systems and its operations

UNIT - IV

Environmental Implications: Environmental standards for Waste to Energy Plant operations and gas clean-up. Savings on non-renewable fuel resources. Carbon Credits: Carbon foot calculations and carbon credits transfer mechanisms

UNIT - V

Case Studies: Success/failures of waste to energy Global Best Practices in Waste to energy production distribution and use. Indian Scenario on Waste to Energy production distribution and use in India. Success and Failures of Indian Waste to Energy plants. Role of the Government in promoting 'Waste to Energy'

TEXTBOOKS:

1. "Industrial and Urban Waste Management in India", TERI Press.
2. Banwari Lal and Patwardhan, "Wealth from Waste: Trends and Technologies" TERI Press.
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