EE-9/2/2021-R&D-E
Government of India
Ministry of Electronics & Information Technology
R&D in Electronics Group
(Microelectronics Development Division)

Dated: 19.05.2023

ADMINISTRATIVE APPROVAL

Subject: Administrative Approval in respect of the project entitled "The Design, Fabrication and Development of Silicon Proven IP Core for High Resolution ADPLL" to be implemented by University College of Engineering Osmania University, Hyderabad and Chaitanya Bharathi Institute of Technology, Hyderabad under Chips to Startup (C2S) Programme.

I am directed to refer to Administrative Approval dated 18.05.2023 for the implementation of Programme "Chips to Startup (C2S) and to convey now the approval of the Competent Authority to the implementation of the above-mentioned project at a total estimated cost of Rs. 191.50 Lakh (Rupees One Crore Ninety One Lakh Fifty Thousand only) as grant-in-aid from Ministry of Electronics and Information Technology. The duration of the project is 5 years. The details of the project are given in the enclosed **Annexure-I**.

2. This issues with the approval of Secretary, MeitY vide computer No. 3080449 dated 03.05.2023 and concurrence of JS&FA, Ministry of Electronics & Information Technology vide computer No. 3080449 dated 03.05.2023.

Meenakshi 19/5/2023

(Meenakshi Kumar)
Under Secretary to Govt. of India

1. The Pay & Accounts Office (PAO), MeitY
2. Office of the Principal Director of Audit, Finance & Communications, Civil Lines, Near Old Secretariat, Shamnath Marg, New Delhi -110 054.
3. Prof. P. Chandra Sekhar, Chief Investigator, Dept. of ECE, Osmania University College of Engineering, Hyderabad, Telangana, 500007
4. Prof. Mohd Ziauddin Jahangir, Chief Investigator, Dept. of ECE, CBIT(A), Gandipet, Hyderabad. 50007
5. DG(NIELIT)/CFO(NIELIT)
6. GC(SV)/GC(AKP)/Sci. 'E'(NG)/Sci. 'D'(HG)/DS(DKS), MeitY
7. Finance Division/HRD/D&D Section, MeitY
8. Master Sanction file.

Annexure-I

1	**Name of the Project**	The Design, Fabrication and Development of Silicon Proven IP Core for High Resolution ADPLL
2	**Objective& Deliverables**	**Objectives:**

1) FPGA Implementation of ADPLL:

- RTL Design and Verification of building block –I of ADPLL: Phase Frequency Detector (PFD) & Time to Digital Converter (TDC).
- RTL Design and Verification of building block –II of ADPLL: Digital Loop Filter
- RTL Design and Verification of building block –III of ADPLL: Digitally Controlled Oscillator (DCO)
- Integration of Building Blocks and Verification of ADPLL.

2) Full Custom IC Design of ADPLL at 180 nm CMOS technology:

- Design, Development and Verification of building block –I of ADPLL: Phase Frequency Detector (PFD) & Time to Digital Converter (TDC)
- Design, Development and Verification of building block –II of ADPLL: Digital Loop Filter.
- Design, Development and Verification of building block –III of ADPLL: Digitally Controlled Oscillator (DCO).
- Integration of Building Blocks and Verification of ADPLL.
- Fabrication and Validation of Full Custom IC Design for ADPLL Functional Verification (Tape Out – 1).
- Fabrication, Testing and Characterization of Full Custom IC Design of ADPLL for complete performance verification (Tape Out – 2).

3) Full Custom IC Design of ADPLL at 90 nm CMOS technology for higher resolution:

- Porting the design, functional and performance validation of the design for 90nm technology.
- Fabrication, Testing and Characterization of Full Custom IC Design of ADPLL for complete performance verification (Tape Out – 3)

4) Development of FM transmitter and receiver using the Fabricated Full Custom ADPLL IC and commercialization of the ADPLL IP.

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Deliverables:

1) Reusable ADPLL ASIC IP
2) FPGA based ADPLL model.
3) Skilled Manpower in the Domain of VLSI
4) PCB based ADPLL Characterization and Debugging board.
5) Sample Application hardware: FM Transmitter/ Receiver using proposed IP.
   Documentation of ADPLL design and characterization results.

3	**Year wise Milestones**	Annexure-A
4	**Name of Implementing Agencies and Legal Status**	**Lead Agency:** Osmania University College of Engineering, Hyderabad -Academic Institute (Govt./State/Autonomous) **Collaborating Agency:** Chaitanya Bharathi Institute of Technology, Hyderabad- Academic Institute (Private/Registered Society/Autonomous)
5.	**Total Project Duration**	5 Years Expected date of commencement: Date of 1st release of GIA Expected date of completion: 5 years from the date of 1st release of GIA

6. Total Project Outlay (GEN Budget Head) : Rs. 191.50 Lakh

A. Cumulative Budget Outlay of the Project (Year wise):

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)					
	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Capital Equipment	15.90	0.00	0.00	0.00	0.00	15.90
Consumable Stores	4.00	4.00	4.00	4.00	4.00	20.00
Duty on Import	1.59	0.00	0.00	0.00	0.00	1.59
Manpower	16.20	24.30	26.76	29.45	32.40	129.11
Travel & Training	3.00	3.00	3.00	3.00	2.93	14.93
Contingencies	1.60	1.60	1.60	1.60	1.60	8.00
Overheads, if any	0.43	0.35	0.39	0.39	0.41	1.97
Grand Total	**42.72**	**33.25**	**35.75**	**38.44**	**41.34**	**191.50**

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B. Agency wise Budget Outlay (Year Wise):

1. Osmania University College of Engineering Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)					
	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Capital Equipment	9.40	0.00	0.00	0.00	0.00	**9.40**
Consumable Stores	2.00	2.00	2.00	2.00	2.00	**10.00**
Duty on Import	0.94	0.00	0.00	0.00	0.00	**0.94**
Manpower	5.40	12.42	13.68	15.05	16.56	**63.11**
Travel & Training	1.50	1.50	1.50	1.50	1.43	**7.43**
Contingencies	0.80	0.80	0.80	0.80	0.80	**4.00**
Overheads, if any	0.15	0.11	0.16	0.14	0.15	**0.71**
Grand Total	**20.19**	**16.83**	**18.14**	**19.49**	**20.94**	**95.59**

2. Chaitanya Bharathi Institute of Technology Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)					
	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Capital Equipment	6.50	0.00	0.00	0.00	0.00	**6.50**
Consumable Stores	2.00	2.00	2.00	2.00	2.00	**10.00**
Duty on Import	0.65	0.00	0.00	0.00	0.00	**0.65**
Manpower	10.80	11.88	13.08	14.40	15.84	**66.00**
Travel & Training	1.50	1.50	1.50	1.50	1.50	**7.50**
Contingencies	0.80	0.80	0.80	0.80	0.80	**4.00**
Overheads, if any	0.28	0.24	0.23	0.25	0.26	**1.26**
Grand Total	**22.53**	**16.42**	**17.61**	**18.95**	**20.40**	**95.91**

7. Implementation Modalities : Osmania University College of Engineering as Lead Agency is responsible for overall implementation of the Project.

8. Mode and extent of funding : **As indicated below:**

(i) Budgetary Support

(a) Grants-in-aid from MeitY : Rs. 191.50 Lakh
(b) Loan : NIL

(ii) Internal generation : NIL

(iii) External Agency, if any : NIL

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9. **Stages of release**

Release No.	**Pre-condition/ Stages**	**Documentation to be supplied by Implementation Agency**	**Amount to be released**
1st release	Initiation of the project	Acceptance of Terms and Conditions governing Grants-in-aid and execution of Memorandum of Understanding (MoU)	Rs. 20.19 Lakh (Osmania University College of Engineering)
			Rs. 22.53 Lakh (Chaitanya Bharathi Institute of Technology)
2nd and subsequent releases	Recommendations of the PRSG & satisfactory progress report of the project	a) Submission of Utilization Certificate of the previous release. b) Technical & Financial Progress Report. **c)** Audited Statement of Accounts (at the time of Project Closure).	Rs. 75.40 Lakh (Osmania University College of Engineering)
			Rs. 73.38 Lakh (Chaitanya Bharathi Institute of Technology)
		Total	**Rs. 191.50 Lakh**

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(Meenakshi Kumar)
Under Secretary to Govt. of India

Annexure A

Year-wise deliverables/Outcomes with specific intermediate milestones

1. Osmania University College of Engineering (A), Nodal Centre

Year	Quarterly Milestones	Timelines	Outcomes
1st	Recruitment and Training of the Project staff and students. Procurement of EDA tools to the institute. Design/Modelling of the System/IP (Delay element &DCO)	Procure the tools and manpower by 2nd month. Model development and proof of concept on FPGA by the year end	Training of the Manpower, Model of the Sub-modules completed.
	RTL Design, Implementation and characterization of Digital Loop Filter on FPGA		
	RTL Design, Implementation, and characterization of Digitally Controlled Oscillator on FPGA		
	Integration of building blocks of ADPLL		
2nd	Validation of the specifications of the System/Subsystem on FPGA and identification of gaps.	Detailed design and development by year end	Detailed design to the Sub-module, meeting the desired specs.
	Design/Modelling of the System/IP (Digital Loop Filter)		
	Design/Modelling of the System/IP(DCO)		
	Integration and functional verification of building blocks of ADPLL		
3rd	Physical Design of Digital Loop Filter	Validation of model for required specs by 9th month	Development of the IP for the sub-module Validated under worst case scenarios.
	Physical Design of DCO		
	Integration of Physical Design of ADPLL and Verification of the System IP for its functionality		
	Verification of the System/subsystem/IP for its performance etc.,		
4th	Tape out- 1(for functional) of the Design @ TSMC 180nm / SCL	By 3rd month, get the IC Characterizing and testing by 6th month. Validation / bug identification	Fabricated IP. Experimental Characterization of the IP Identification of Bugs
	Development of Prototyping Board (for characterization and testing)		
	Tape out-2 (complete specs.) of the Design @ TSMC 180nm / SCL. Testing& Characterization		
	PCB prototype of ADPLL Characterization and Debugging board		
5th	Tape out of the Design @ TSMC 90nm (if required) for higher resolution, Testing& Characterization	Completing iteration if	Fabricated IP.

	Validation of the subsystem/IP of the Proposed work	required by the 6th month.	Experimental Characterization of the IP. Commercialization of IP
	Development of FM transmitter using IP, Field trials and deployment		
	commercialization plans of the technical outcomes.		

2. Chaitanya Bharathi Institute of Technology(A)(Participating Institute)

Year	Quarterly Milestones	Timelines	Outcomes
1st	Recruitment and Training of the Project staff and students. Procurement of EDA tools to the institute. Design/Modelling of the subsystem/IP (TDC, ADPLL)	Procure the tools and manpower by 2nd month. Model development and proof of concept on FPGA by the year end	• Training of the Manpower, • Model of the Sub-modules completed.
	RTL Design, Implementation and characterization of TDC on FPGA		
	RTL Design, Implementation, and characterization of Delta-Sigma Modulator on FPGA		
	Integration of building blocks of ADPLL		
2nd	Validation of the specifications of the System/Subsystem on FPGA and identification of gaps.	Detailed design and development by year end	• Detailed design to the Sub-module, meeting the desired specs.
	Design/Modelling of the System/IP (TDC)		
	Design/Modelling of the System/IP(DSM)		
	Integration and functional verification of building blocks of ADPLL		
3rd	Physical Design of TDC	Validation of model for required specs by 9th month	• Development of the IP for the sub-module • Validated under worst case scenarios.
	Physical Design of DSM		
	Integration of Physical Design of ADPLL and Verification of the System IP for its functionality		
	Verification of the System/subsystem/IP for its performance etc.,		
4th	Tape out- 1(for functional) of the Design @ TSMC 180nm / SCL	By 3rd month, get the IC Characterizing and testing by 6th month. Validation / bug identification	• Fabricated IP. • Experimental Characterization of the IP • Identification of Bugs
	Development of Prototyping Board (for characterization and testing)		
	Tape out-2 (complete specs) of the Design @ TSMC 180nm / SCL. Testing& Characterization		
	PCB prototype of ADPLL Characterization and Debugging board		

5th	Tape out of the Design @ TSMC 90nm(if required) for higher resolution, Testing& Characterization	Completing iteration if required by the 6th month.	• Fabricated IP. • Experimental Characterization of the IP. • Commercialization of IP
	Validation of the subsystem/IP of the Proposed work		
	Development of FM transmitter using IP, Field trials and deployment		
	commercialization plans of the technical outcomes.		