CHAITANYA BHARATI INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Stake holder involvement in Curriculum Development

AY 2018-19

Action taken and implementation in Curriculum

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DEPARTMENT OF ECE
Chaitanya Bharathi Institute of Technolog
Hyderabad-500 075

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1) Industry

S.no.	Suggestions & opinion	Actions Taken
1.	Apart from INTEL Microcontroller Architecture, Advanced Microcontroller architecture of ARM can be included in the subject microcontroller.	It is a core course and enough care is taken while drafting the syllabus. This lab course is introduced in the curriculum.
2.	Less focus on Exponential Fourier Series in the subject "Signal and Systems" is noticed.	These topics are included in the syllabus.
3.	Less Weightage for applications of multirate DSP in the subject digital signal processing is found.	It is included in the syllabus

1) Industry (Proofs)

18ECC21

MICROCONTROLLERS

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	70 Marks
CIE	30 Marks
Credits	3

Prerequisite: Knowledge of Computer Architecture and Microprocessors.

Course Objectives:
This course aims to:

1. Understand architecture features of the microcontrollers
2. Learn the programming of the microcontrollers
3. Understand interfacing of various modules with microcontrollers.

Course Outcomes:
Upon completion of this course, students will be able to:

1. Acquire an overview of how a processor and a controller are distinguished.
2. Understand the architectures of different microcontrollers to enable to design applications using them.
3. Develop code both in assembly and in high level language for various applications of microcontrollers.
4. Analyze and design real world applications by using on/off chip peripherals of different microcontrollers.
5. Apply theoretical learning to practical real time problems for automation.

UNIT-I
8051Microcontroller: Introduction to Microcontroller, Overview of 8051 family, Internal Architecture of 8051, PSW, Pin description, I/O Ports, Memory organization and expansion. Addressing modes and Bit addressable features, 8051 Instruction set: Data transfer, Arithmetic, Logical, Program branching and bit manipulation instructions.

UNIT-II
8051 Programming: Introduction to 8051 programming development tools, basic programming using instruction set, Introduction to 8051 C Programming, SFRs, 8051 Timer Programming in Assembly and C, 8051 Serial port Programming in Assembly and C, 8051 Interrupt Programming in Assembly and C.

UNIT-III
8051 Interfacing: 8051 interfacing to external memory (RAM, ROM), 8255 PPI interfacing, LCD and Keyboard interfacing, Digital to Analog converter, Analog to Digital converter and Sensor interfacing, Relay and PWM, DC Motor interfacing, Stepper Motor interfacing

UNIT-IV
ARM: Introduction to RISC Processors, ARM Design Philosophy, ARM Processor families, Architecture- Revisions, Registers, Program status register, Pipeline, Introduction to Exceptions,
ARM Instruction set: Data processing instructions, Branch instructions, Load-Store instructions, Software interrupt instruction, Program Status Register instructions, Loading constants, and Conditional executions. Introduction to THUMB instructions: Differences between Thumb and ARM modes, Register usage.

UNIT-V
ARM 7 Microcontroller (LPC2148): Salient features of LPC 2148, Pin description of 2148, Architectural Overview.
ARM 7(LPC2148) **Peripherals:** Description of General-Purpose Input/output (GPIO) ports, Pin control Block. Features, Pin description, Register description and operation of PLL, Timers, PWM, ADC, DAC. Communication protocols: Brief overview on I2C, SPI, and CAN.

18EC C04

SIGNALS AND SYSTEMS

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	70 Marks
CIE	30 Marks
Credits	3

Prerequisite: Knowledge of Differential and Integral Calculus.

Course Objectives:
This course aims to:
1. Know Signals and systems representation/classification, time and frequency domain analysis of continuous time signals with Transform techniques.
2. Expose Sampling, time and frequency domain analysis of discrete time signals with DTFT and Z-Transforms.
3. Familiarise concepts of convolution and correlation integrals.

Course Outcomes:
Upon completion of this course, students will be able to:
1. Classify signals, systems and analyze them using Transform techniques.
2. Evaluate signal characteristics using time and frequency domain analysis.
3. Assess the systems stability and causality
4. Describe the Sampling process and analyze the DT Signals/Systems using DTFT and Z Transform.
5. Apply the Convolution and correlation concepts for analysis of signals and systems

UNIT-I
Continuous Time Signals:
Introduction to signals, their representations and classification. Introduction to systems and their classifications, Orthogonality of signals, Complete set of mutually orthogonal signals, Harmonic signals.
Signal Representation:
Exponential Fourier series, Existence and Convergence. Symmetry conditions, Amplitude and Phase spectra. Power Spectral Density.

UNIT-II
Fourier Transforms:
The direct and inverse Fourier transforms, Existence, Frequency spectrum and properties of Fourier Transforms, Fourier Transform of singularity functions and periodic signals. Energy Spectral Density, Filter characteristics of linear systems, Distortion less system, Phase delay and group delay.

UNIT-III
Signal Representation by Generalized Exponentials:
The Bilateral and unilateral Laplace transforms. Region of convergence and its properties. Properties of Laplace transform, Inverse Laplace transform, Laplace transform of periodic signals. **LTI system:** Impulse response, System transfer function, Stability and Causality.

UNIT-IV
Discrete Time Signals:
Sampling of continuous time signals, DTS representation. Discrete Time Fourier Transform and properties.
Z–Transform: The Direct Z-Transform, Region of convergence and its properties. S–Plane and Z–Plane correspondence, Z–Transform properties. Inverse Z–Transform, Discrete LTI system: impulse response and system transfer function. Stability and Causality.

18EC C20

DIGITAL SIGNAL PROCESSING

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	70 Marks
CIE	30 Marks
Credits	3

Prerequisite: Concepts of Signals, Systems and Filter designing.

Course Objectives:
This course aims to:

1. Know Discrete-time signals in the frequency domain using DFT and FFT.
2. Design digital IIR and FIR filters for the given specifications.
3. Introduce the basics of Multirate digital signal processing, Digital signal processor and its applications

Course Outcomes:
Upon completion of this course, students will be able to:

1. Understand the concept of DFT and FFT for signal processing applications.
2. Design FIR filters for the given specifications.
3. Implementation of IIR filters for the given specifications.
4. Interpret the concepts of Multirate digital signal processing and its applications.
5. Explain the architecture features of TMS320C67XX processor.

UNIT-I
Discrete Fourier Transform: Introduction, Discrete Fourier Transform (DFT), Properties of DFT, Efficient computation of DFT-Fast Fourier Transform (FFT) algorithms: Radix-2 FFT algorithms – Decimation in Time, Decimation in Frequency algorithms, Inplace computation, Bit reversal algorithm, Linear filtering using FFT algorithm.

UNIT-II
FIR Filter Design: Amplitude and Phase responses of FIR filters – Linear phase FIR filters – Windowing technique for design of FIR filters – Rectangular, Bartlet, Hamming, Blackman, and Kaiser Windows. Realization of digital filters-Direct form-I and II of IIR filters, Realization of linear phase FIR filter, Finite word length effects.

UNIT-III
IIR Filter Design: Butterworth and Chebyshev approximation, IIR digital filter design techniques- Impulse Invariant transformation, Bilinear transform techniques, Digital Butterworth and Chebyshev filters, Spectral transformation techniques. Comparison between FIR and IIR filters.

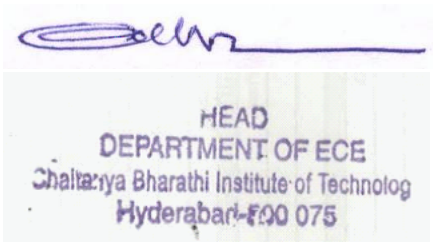
UNIT- IV
Multirate Digital Signal Processing: Introduction -Decimation by a Factor -D, Interpolation by a Factor -I, Sampling Rate Conversion by a Rational Factor -I/D, Nobel identities, Applications of Multirate Signal Processing: Phase shifters, QMF filter banks, Narrowband filters and sub band coding of speech signal.

UNIT-V
DSP Processors: Introduction, Difference between DSP and General-Purpose Processor architectures, need for DSP processors. General purpose DSP processor- TMS320C67XX processor, architecture, functional units, pipelining, registers, linear and circular addressing modes, instruction set.

2) Alumni

S.no.	Suggestions & opinion	Action taken
1.	In Computer Architecture and Microprocessors I have noticed that to Analyze the Computer architecture concepts, an application is needed to be in corporates as any architecture of the processor.	8086 processor is included in the syllabus
2.	In Coding Theory and Techniques, importance of decoding algorithm is missing. Priority must be given to the codes based on abstract algebra.	The topics are added in the syllabus

2) Alumni (Proof)



18ECC15

COMPUTER ARCHITECTURE AND MICROPROCESSORS

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	70 Marks
CIE	30 Marks
Credits	3

Prerequisite: Basic knowledge on digital system design

Course Objectives:
This course aims to:
1. Study and understand the principles of computer system
2. Understand the design of computer system
3. Explore the architecture and instruction set of the microprocessors

Course Outcomes:
Upon completion of this course, students will be able to:
1. Understand how computer works.
2. Apply fixed and floating-point arithmetic algorithms.
3. Compare various memories, memory access techniques.
4. Assess the performance of computers.
5. Analyze architecture and instruction set of microprocessors.

UNIT-I
Data representation and Computer Arithmetic: Basic structure of computers, Functional units, Fixed point representation of numbers, Digital arithmetic algorithms for Addition, Subtraction, Multiplication using Booth's algorithm and Division using restoring and non-restoring algorithms, Floating point representation with IEEE standards.

UNIT-II
Basic Computer Organization and Design: Instruction codes, Stored program organization, Computer registers and computer instructions, Timing and control, hardwired and micro programmed control unit, Instruction cycle, Program interrupt, Interrupt cycle, Micro programmed Control organization, Address sequencing, Micro instruction format.

UNIT-III
Central Processing Unit: General register organization, Stack organization, Instruction formats, Addressing modes, Data transfer and manipulation, Program control, CISC and RISC: features and comparison, Instruction Pipeline.
Input-Output Organization: Peripheral devices, I/O interface: I/O Bus and interface modules, isolated versus memory mapped I/O. Modes of Transfer: Programmed I/O, DMA and Interrupt initiated I/O. Priority interrupt: Daisy chaining, Parallel Priority interrupt

UNIT-IV
Memory Organization: Memory hierarchy, Primary memory, Auxiliary memory, Associative memory, Cache memory, mapping functions: direct, associate and set associate, Virtual memory: address mapping using pages, Memory management.

UNIT-V
8086 Microprocessor: Evolution of microprocessors, 8086 Microprocessor: Internal architecture, flag register, Signal description under minimum and maximum mode of operation, register organization, Addressing modes. Overview of Instruction set. Introduction to the advanced microprocessors (x86): Salient features, real and protected modes. Evolution of Pentium Processors.

18EC E10
CODING THEORY AND TECHNIQUES

(Program Elective-III)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	70 Marks
CIE	30 Marks
Credits	3

Prerequisite: Student must have completed the course in Digital communication.A good background of mathematics including probability theory is expected.

Course Objectives:
This course aims to:

1. Implementation of channel coding techniques in digital communications.
2. Know basic notions of error control coding and fundamentals of abstract algebra, finite fields and its extension.
3. Understand the mathematical structure and algorithms for RS and BCH codes.

Course Outcomes:
Upon completion of this course, students will be able to:

1. Recall the theory and principles of information theory and channel Coding.
2. Design and analyze the encoding and decoding circuits for various coding techniques.
3. Apply the principles of abstract algebra, finite fields and its extension to design related codes.
4. Examine the error detection and correction capability of coding techniques for digital communication.
5. Evaluate the performance of error control codes using different decoding algorithms

UNIT-I
Linear Block Codes: Introduction, generator and parity-check matrices, encoding, Syndrome decoding, Maximum Likelihood (ML) decoding-hard decision decoding and soft decision decoding.
Binary Cyclic Codes: Description, encoding, Syndrome computation and error detection, Encoder and Syndrome generator implementations, Meggit decoder.

UNIT II
Galois Fields: Fields, Binary arithmetic, Basic properties of Galois Fields, polynomials over GF (2), Construction of Galois Fields $GF(2^m)$ from GF (2), properties of extension fields, conjugates, Minimal polynomials, Factorization of (X^n+1) over a finite field.

UNIT III
BCH Codes: Introduction, general description of BCH codes, Encoding, Decoding – Berlekamp's algorithm, a Fast Berlekamp-Massey algorithm.

UNIT IV
RS Codes: Introduction, general description of Reed-Solomon codes, encoding, decoding of Reed- Solomon codes using Berlekamp-Massey algorithm. MDS codes, Spectral characteristics of cyclic codes.

UNIT V
Convolution Codes: Introduction, Encoding, State diagram, Code Tree, Code Trellis diagram, Decoding -Wozencraft's sequential decoding, Fann's algorithm, Maximum Likelihood (ML) Viterbi decoding - soft decision and hard decision decoding.

3) Parent

S.no.	Suggestions &opinion	Action Taken
1.	Introduce a course on current trending topics such as Block chain technology, cryptography and Cyber security	Cryptography and Block chain Technology is included as PE-IV in VII Semester

3) Parent (proof)

CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (A)

AICTE Model Curriculum with effect from AY 2021-22

B.E (Electronics and Communication Engineering)

List of Courses in Program Elective-IV		List of Courses in Program Elective-V		List of Courses in Open Elective-II	
Course Code	Title of the Course	Course Code	Title of the Course	Course Code	Title of the Course
18ECE15	Cryptography and Blockchain Technology	18ECE20	CMOS RF IC Design	18CE O02	Disaster Mitigation and Management
18ECE16	DSP Processors and Architectures	18ECE21	Digital Image Processing	18ME O04	Entrepreneurship
18ECE17	Principles of Computational Electromagnetics	18ECE22	Embedded Systems	18CS O06	Fundamentals of DBMS
18ECE18	Semiconductor Memory Design and Testing	18ECE23	Software Defined Radio	18IT O02	Python Programming
18EC E19	Speech Processing	18EC E24	5G Communications	18EG O01	Technical Writing Skills

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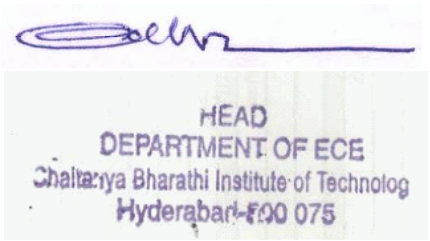
4) Faculty feedback

S. no	Suggestions/Feedback	Action Plan
1.	In Network Theory, include topics on network analysis and network synthesis. Also include topics on symmetrical and asymmetrical network properties and analysis.	The topics are added in the syllabus
2.	In Principles of GNSS, IRNSS architecture, signals, limitations and advantages may be included	It is included in VII semester
3.	In CAMP course 8086 microprocessor architecture and memory organization to analyze the computer architecture concepts may be included.	It is included in VI Semester

4) Faculty feedback (proof)



18EC C03

NETWORK THEORY

Instruction	3 L Hours per week
Duration of SEE	3 Hours
SEE	70 Marks
CIE	30 Marks
Credits	3

Prerequisite: Knowledge on Elements of Electrical Engineering.

Course Objectives:
This course aims to:
1. Make understand the concepts of Electric Circuits, Network Theorems and the transients.
2. Make understand the concept of steady state and applying phasor analysis to AC circuits and analyzing magnetic coupled circuits.
3. Familiarize resonant circuits, two port network parameters, concept of Passive Filters and Network Synthesis.

Course Outcomes:
Upon completion of this course, students will be able to:
1. Recall basics of electrical circuits with nodal and mesh analysis
2. Illustrate electrical theorems for AC and DC Circuits.
3. Perform time domain and frequency domain analysis for networks.
4. Analyze the electrical network and two port network parameters for different applications i.e., magnetic coupled circuits, Filters.
5. Build different networks using various synthesis methods.

UNIT-I
Network Theorems: Network reduction techniques, Super Nodal and Super Mesh Analysis, Superposition, Thevenin's and Norton's theorems. Reciprocity, Maximum Power Transfer, Compensation, Millman's, Duality and Tellegen's Theorems using dependent and independent sources.

UNIT-II
Transients: Introduction, Study of initial conditions, DC transients RL, RC circuits, RLC circuits, Formulation of integral, differential equations. Circuit analysis using Laplace Transform and inverse Laplace Transform, Pole-Zero Plots, Zero Input Response, Zero State Response.

UNIT-III
Steady State Analysis of AC circuits: Phasor and vector representations, impedance and admittance, Average power, Apparent Power, Complex Power, Power triangle.
Coupled circuits: Concept of self, mutual inductance, co-efficient of coupling, dot convention rules and analysis of simple circuits.

UNIT-IV
Frequency Domain Analysis: Concept of complex frequency, impedance and admittance functions, Series and parallel resonance, Q-factor, selectivity, bandwidth.
Two Port Networks: Z, Y, h, g, ABCD and Inverse ABCD parameters, equivalence of two port networks. Interconnection of two port networks.

UNIT-V
Filters: Introduction to Filters and classification of Filters (Low pass, High pass, Band pass and Band stop) and their design aspects. **Network Synthesis:** Elements of circuit synthesis, Foster and Cauer forms of LC Networks, Synthesis of RC and RL networks.

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18ECE26

PRINCIPLES OF GNSS

(Program Elective-VI)

Instruction	3 L Hours per Week
Duration of SEE	3 Hours
SEE	70 Marks
CIE	30 Marks
Credits	3

Prerequisite: Fundamental concepts of communication are required.

Course Objectives:

This course aims to:

1. Explain the basic principle of operation of GPS, GPS ephemerides and signal structure.
2. Make the students to understand various coordinate systems and highlight the effect of various errors affecting GPS signals.
3. Make the students to appreciate the significance of other GNSS systems, principle of DGPS and augmentation systems.

Course Outcomes:

Upon completion of this course, students will be able to:

1. Demonstrate the fundamental concepts of communications in understanding of GPS architecture, operation and signal structure.
2. Apply the principles of orbital mechanics, time references, coordinate systems and range measurements in estimating user position.
3. Examine the effect of various error sources and satellite geometry on position estimates and analyze the suitability of a given data format.
4. Compare the architecture and working of other GNSS systems and make use of GNSS systems in a variety of civilian and defense applications.
5. Relate the knowledge of DGPS techniques in understanding augmentation systems.

UNIT-I

GPS Fundamentals: GPS System Segments: space, control and user segments, Principle of operation, Current status of GPS satellite constellation. Orbital Mechanics: GPS ephemeris data, algorithm for computation of satellite's position from ephemeris data. Time References: solar and sidereal days, UTC time, GPS time.

UNIT-II

GPS Signals: Legacy GPS signals: Signal structure, Operating frequencies, C/A and P-Code, Navigation message, Modernized GPS signals: list of signals and their significance. Range measurements: code and carrier measurements, User position estimation with PRN codes.

Coordinate systems: Earth Centered Earth Fixed (ECEF) coordinate system, Earth Centered Inertial (ECI) coordinate system, Geodetic coordinate system, Ellipsoid and Geoid, Regional and Global Datum, World Geodetic System (WGS-84).

UNIT-III

GPS Error Sources: Satellite clock error, ephemeris error, Receiver clock errors, satellite and receiver instrumental bias, Multipath error, receiver measurement noise, ionospheric error and tropospheric error, Klobuchar model, ionospheric delay estimation using dual frequency measurements and UERE. Dilution of precision: HDOP, VDOP, TDOP, PDOP & GDOP.

UNIT-IV

Data Formats: RINEX Observation and Navigation Data formats

GNSS: Architecture, operation and signals of other global navigational satellite systems Galileo, Beidou and GLONASS.

IRNSS: Architecture, signals, limitations and advantages.

18ECC15

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