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|---|---|---|
| Name of Faculty | Dr.B.KHALEELU REHMAN | |
| Designation | Associate Professor | |
| Nature of Job/Appointment | Regular | |
| Date of Joining | 16 - 12 - 2022 | |
| E-mail | khaleelurehmanb_ece@cbit.ac.in | |

| Education Qualifications | Name of the Degree | Class |
|---|---|---|
| Ph. D | Doctor of Philosophy (ECE) | Awarded |
| PG | M. Tech. (VLSI Design ) | Distinction |
| UG | B. Tech. (ECE) | First Class |

| Work Experience | |
|---|---|
| Teaching | 14.8 Years |
| Research | 05 years |
| Industry | -- |
| Others | -- |
| Area of Specialization | VLSI Design, Signal Processing |
| Professional Memberships | Member, International Association of Engineers - IAENG |
| Responsibilities held at Institution Level | -- |
| Responsibilities held at Department Level | 1. Industry Institute coordinate cell coordinator in Nalla Malla Reddy Engineering college(Autonomous) during 2020-2021 and 2021-22<br>2. BOS member in Nalla Malla Reddy Engineering college(Autonomous)<br>3. PG coordinator for VLSI Design in Nalla Malla Reddy Engineering college(Autonomous)<br>4. Member, Course Expert Group. |
| Research Guidance | 1. 01 Research scholar pursuing Ph.D. from Lincoln University College, Malaysia |
| Awards Received | 1. Certificate of Appreciation from R & D department, UPES, Dehradun, in event R & D Research Award Ceremony 2018 for publishing research papers during the Academic year 2017-2018.<br>2. Certificate of Appreciation from R & D department, UPES, Dehradun, in event R & D Research Award Ceremony 2017 for publishing research papers during the Academic year 2016-2017. |
| Courses Handled at Under Graduate / Post Graduate Level. | Digital system Design, VLSI Design, Signals and Systems, Digital Signal Processing, Electronic Devices and Circuits, Test and Testability, Analog and Digital Electronics, Basic Electronics. |
| No. of Papers Published | National Journals – -- International Journals – 17<br>National Conference – 01 International Conference – 09 |
| Projects Carried out | -- |
| Patents | Application Number : 2018110079990A<br>Title of the Invention :Method and system to detect crack in Rail Track Date of Publishing : 05.03.2018 |

| Technology Transfer | -- |
|---|---|
| Invited Speaker | 1. Keynote speaker on the topic "Xilinx IP cores and its applications" one week FDP organized by "J.B.Institute of Engineering & Technology, Hyderabad from 29th Nov-4th Dec 2021. |
| | 2. Resource person on the topic "Recent Trends in Electronics and Communication Engineering" One week FDP organized by "J.B.Institute of Engineering & Technology, Hyderabad from 26th April-2nd May 2020. |
| | 3. Keynote speaker on the topic "Emerging Trends in Electronics and Communication Engineering" One week FDP organized by "Nalla Malla Reddy Engineering College Hyderabad from 05th June-10th June 2020 |
| | 4. Keynote speaker on the topic "Emerging Trends in Electronics and Communication Engineering" One week FDP organized by "Nalla Malla Reddy Engineering College Hyderabad from 05th June-10th June 2020 |
| | 5. Guest lecture on the topic "MATLAB and its applications on physics" organized by Govt. College for men on 09th January, 2019 at Kurnool. |
| | 6. Guest lecture on the topic "Job opportunities in Electronic industry" organized by Govt. College for men on 04th January, 2018 at Kurnool. |
| | 7. Session Chair- 1st International Conference on Intelligent Communication, Control and Devices (ICICCD-2016), Dehradun, India, 2016 (Springer Conference) |
| | 8. Session Chair- 2nd International Conference on Intelligent Communication, Control and Devices (ICICCD-2017), Dehradun, India, 2017 (Springer Conference). |
| | 9. Session Chair- Global Emerging Innovation Summit 2021(GEIS 2021), Organized by Lovely Professional University, Punjab (Bentham Science Publication Partner). |
| | 10. Reviewer for Tech Science press journals(SCI and Scopus Indexed) |
| No. of Books/Chapter Published with details | 1. **B.KhaleeluRehman**,Vallathan,Vetriveeran,Salauddin,(2022).Xilinx FPGA and Xilinx IP Cores: A Boon to curb Digital Crime" Digital Forensics and Internet of Things: Impact and challenges,(131-162) © 2022 Scrivener Publishing LLC.<br>2. **B.KhaleeluRehman**,Isaac,Munaf,Salauddin,Mudasar Basha.(2022).FPGA Implementation of Area-efficient binary counter using Xilinx IP cores in Lecture Notes in Civil Engineering, Vol. 199.Chapter-14,Springer Nature. |
| Details of Short-Term Training Programs/Faculty Development Programs/Seminars/Workshops. Other Trainings (**Attended and/or Organized**). | 1. Successfully Organized a One Week Faculty Development Program on "Emerging Trends in Electronics and Communication Engineering "during 05-10th June 2020 in Nalla Malla Reddy Engineering College (Autonomous), Hyderabad.<br>2. Successfully Organized a One Week Professional Software Training, "Application of MATLAB on Signal Processing Level-1" during 17-23rd Dec 2018 in University of Petroleum & Energy Studies, Dehradun.<br>3. Successfully Organized a One Week Professional Software Training, "Digital system Design using VHDL" during 18-24th May 2018 in University of Petroleum & Energy Studies, Dehradun<br>4. Successfully Organized a One Week Professional Software Training, "Application of MATLAB on Signal Processing Level- |

1" during 12-17th Dec 2016 in University of Petroleum & Energy Studies, Dehradun.

5.  Successfully Organized a three day workshop on  Network Security & Ethical Hacking during 07-09th November 2014 in University of Petroleum & Energy Studies, Dehradun

6.  Successfully completed a 10 days FDP on Application of Machine learning in Electronics and Communication Engineering by E&ICT, NIT-Warangal during 7th March to 16th March 2022.

7.  Successfully completed a 15 days Certification course on CISCO "Introduction to networks & Routing and Switching essentials" in Amity University, Noida during 16th Aug-02nd Sep, 2016.

8.  Successfully completed a 15 days training on "Advanced VLSI and Embedded system design" by Unistring Technologies, Hyderabad.  During 10thJuly-22rd July 2017.

9.  Successfully completed a 15 days training on   backend tools on VLSI Design by LeadSoc Technologies India Pvt limited, Bangalore during 24th Dec 2018-08th Jan 2019.

10. Successfully completed a 15 days course on Winter School on Digital VLSI design (WSDVD) by IETE, Ranchi during 16th Dec to 31st Dec, 2015.

11. Successfully completed 2 Weeks ISTE Workshop on Control Systems by IIT Kharagpur during 2nd to 12th Dec 2014.

12. Successfully completed one week FDP on "VLSI DESIGN" by NITTTR, Chandigarh during 10th- 14th March, 2014.

13. Successfully completed  AICTE sponsored Short term course on "Computational Methods in Signal Processing and Machine Learning" by  QIP CENTER ,INDIAN INSTITUTE OF TECHNOLOGY INDORE during 14th-19th Dec,2020

14. Successfully completed   5 day FDP on "Fragrance of signal processing" by  Department of ECE , V.K.R,V.N.B & A.G.K college of Engineering, Gudivada during 10th-14th July,2020

15. Successfully completed AICTE sponsored one week workshop on Emerging trends in VLSI Technology, by Malla Reddy Engineering College for Women, Hyderabad. During 22nd to 27th March 2021.

16. Successfully completed IIEECP Phase-1 IUCEE International Engg Educator Certification Program by  Nalla Malla Reddy Engineering College (Autonomous), Hyderabad. During 12th-19th Jan 2021.

17. Successfully completed Two days workshop on "CMOS Layout Design Flow uses Microwind Tool" by JNTUH and TechFLUENT Solutions Pvt. Ltd, Hyderabad. During 02nd September to 03rd September 2022.

18. Successfully completed a 5 day Workshop on Fundamentals of Digital World by Nalla Malla Reddy Engineering College (Autonomous), Hyderabad. During 17th April to 26th April 2021.

19. Successfully completed two day workshop on Accelerating project based learning using Internet of Things and Thing speak, by Regional Research symposium on PBL-2021 During18th and 19th June 2021.

20. Successfully completed 5 days training on "Open Source Software Training & Awareness (LATEX)" by University of Petroleum & Energy Studies, Dehradun. During 29th Jan 2019 -02nd Feb 2019

21. Successfully completed two day's workshop on Wind River's "VxWorks" RTOS software Training organized by University of Petroleum & Energy Studies, Dehradun. During 12th Jan 2016 - 13th  Jan 2016

22. Successfully completed two day's workshop on Basics of HFSS by ANSYS (Antenna, RF design and Microwave Components) at University of Petroleum & Energy Studies, Dehradun. During 17th March 2018 -18th March 2018.

23. Successfully completed one day Webinar on Artificial Intelligence IC's organized by B.V Raju Institute of Technology, Hyderabad. On 19th Dec2020.
24. Successfully completed one day Workshop on "Analog IC Design Using Mentor EDA Tools" Organized by Corel Technologies and Mentor on 10th April, 2020
25. Successfully completed one day Workshop on "Custom IC Design and Validation using Xilinx Vivado"" Organized by Corel Technologies and Mentor on 22nd May, 2020
26. Successfully completed one day Workshop on Functional Verification using Cadence Incisive tool" Organized by Entuple Technologies on 20th May, 2020.
27. Successfully completed one day workshop on Innovation on National Education policy (NEP) innovation & Entrepreneurship Organized by B.V Raju Institute of Technology, Hyderabad. On 29th Nov, 2020.
28. Successfully completed one day workshop on Intellectual Property Rights: Technology Development and Its Commercialization (IPRTDC-2019) Organized by University of Petroleum & Energy Studies, Dehradun on 28th August 2018.
29. Successfully completed one day workshop on "Technical Writing using Latex" Organized by University of Petroleum & Energy Studies, Dehradun on 24th October , 2015

Details of Journal Publications/ Conferences (**National and International**)

**International Journals:**

1. Adesh Kumar, Gaurav Verma, Mukul Kumar Gupta, **B. Khaleelu Rehman**, Mohammad Salauddin, Deepak Kumar "3D Multilayer Mesh NoC Communication and FPGA Synthesis" Wireless Personal Communications, Springer, 2018, doi: 10.1007/s11277-018-5724 (SCI Indexed, Scopus Indexed)
2. **B.Khaleelu Rehman** ,Adesh Kumar, Paawan Sharma, "A Novel approach for R- Peak detection in the Electrocardiogram(ECG) signal" ARPN Journal of Engineering and Applied Science(JEAS) ,December 2016,Volume 11 number 21 , Page(s): 13500 – 13503,ISSN-1819-6608. (Scopus Indexed)
3. **B.Khaleelu Rehman**, Adesh Kumar, Paawan Sharma "Comparative study of high performance QRS complex detection on Electrocardiogram signal". International Journal of control theory and applications (IJCTA). Volume: No.10 (2017) Issue No. : 7 (2017).Pages 111-120. ISSN: 0974-5572 (Scopus Indexed).
4. **B. Khaleelu Rehman**, Adesh Kumar, and Paawan Sharma "A FPGA based High performance heart beat monitoring system". International Journal of control theory and applications (IJCTA). Volume: No.10 (2017) Issue No. : 18 (2017).Pages 245-253. ISSN: 0974-5572. (Scopus Indexed).
5. **B. Khaleelu Rehman**, Adesh Kumar, and Paawan Sharma. "Modeling and Simulation of ECG Signal for Heartbeat Application. "Advances in Intelligent Communication, Control and Devices, pp. 503-511. Springer, Singapore, 2018. (Scopus Indexed).
6. Mohammad, Salauddin, Madan Gopal, Raja Rao Manda, and **B.Khaleel Rehman**. "Mitigation of Signal Interference by Positioning FFT Window for OFDMA System." In Intelligent Communication, Control and Devices, Advances in Intelligent Systems and Computing, pp. 561-568. Springer, Singapore, 2018. (Scopus indexed)
7. Basha, Mudasar, M. Siva Kumar, Vemulapalli Sai Pranav, and **B. Khaleelu Rehman**. "Approach to Find Shortest Path Using Ant Colony Algorithm." In Intelligent Communication, Control and Devices, Advances in Intelligent Systems and Computing pp. 1243-1252. Springer, Singapore, 2018. (Scopus indexed)
8. Reddy, K. Venkata Siva, P. Vishnu Kumar, K. Maheswari, and **B. Khaleelu Rehman**. "Design and Verification of 16-Bit Vedic Multiplier Using 3: 2 Compressors and 4-Bit Novel Adder." In Proceeding of International Conference on Intelligent Communication, Control and Devices, Advances in Intelligent Systems and Computing pp. 723-732. Springer, Singapore, 2017. (Scopus indexed).
9. Mohammad, Salauddin, R. Seetha, S. Jayamangala, **B. Khaleelu Rehman**, and D. Kumar. "Implementation of FM-Based Communication System with 3-Level Parallel Multiplier Structure for Fast Transmission Using

FPGA." In Intelligent Communication, Control and Devices, pp. 619-626. Springer, Singapore, 2019.( Scopus indexed).

10. **B.Khaleelu Rehman**, Adesh Kumar, Salauddin Mohammad, Mudasar Basha, and K. Venkata Siva Reddy. "Detection of DTMF by Using Goertzel Algorithm and Optimized Resource-Sharing Approach." In Intelligent Communication, Control and Devices, pp. 851-856. Springer, Singapore, 2019.( Scopus indexed).

11. Shubhankar Thapliyal , Kartik Sehgal , Utkarsh Sundaram, Akshay Sharma , **B Khaleelu Rehman** "Designing an Improved 64 Bit Arithmetic and Logical Unit for Digital Signaling Processing Purposes" International Scientific Research Organization Journal, Volume 02 Issue 01, 2017, e-ISSN- 2455–8818.

12. Sana parween, Madhurima, **B.Khaleelu Rehman** "A Novelty techniques for noise removal in ECG signals "International Journal of Electrical, Electronics & Computer Science Engineering (E2CE-2016), 2016 12-13 August 2016 , Page(s): 14 – 16,Specail issue  Print ISBN: 2454-1222, Online ISBN:2348-2237.

13. Hussai, Beporam Iftekhar, Mir Safiulla, and **B. Khaleelu Rehman**. "Application of Rapid Tooling for Vacuum Forming to Reduce Cycle Time." In Advances in Fire and Process Safety, pp. 243-251. Springer, Singapore, 2018.

14. **B. Khaleelu Rehman**, Salauddin Mohammad, Mudassar Basha "Implementation of 3bit parallel adder using XILINX IPCORES A Case Study" Journal of VLSI Design Tools & Technology,2020

15. **B.khaleelu Rehman**,Mudasar Basha,Mohammad Waaiz,Mohammad Salauddin" "Hardware implementation of parallel adder/Subtractor and complex multiplier using Xilinx IP core" International Journal of Technology, Management & Knowledge Processing,2021

16. Sai Maadhav Madderla, Kaushik Kumar K N, Satya Durga P**, Dr.B.Khaleelu Rehman** "AI and ML based Product label and text reading System." International Journal of Engineering Research and Applications (IJERA), vol.12 (06), 2022, pp 07-13.

17. B **Khaleelu Rehman**, Navya, Naveen, T.Rajani, Shivaranjani. "FPGA implementation of ECG signal characteristics", International Journal of Engineering Development and Research (IJEDR), ISSN:2321-9939, Vol.10, Issue 3, pp.41-46, July 2022

### International Conference Publications  :

1. **B.Khaleelu Rehman**, Adesh Kumar, Salauddin Mohammad B.Iftekhar Hussain. "High Performance Real time ECG Signal Processing System" 2nd   International Conference on Doctoral Colloquium, Dehradun , Uttarakhand, India, May 2019.

2. Salauddin Mohammad, **B. Khaleelu Rehman**, K.snehalata, B.Soumya. "Viability of comb filter for hearing impaired through FPGA" 2nd   International Conference on Doctoral Colloquium, Dehradun, Uttarakhand, India, May 2019.

3. B. Iftekhar Hussain**, B.Khaleelu Rehman,** "Application of Engineering Economics for implementing rapid tooling in a plastics forming firm" 2nd   International Conference on  Doctoral Colloquium, Dehradun,Uttarakhand,India,May 2019.

4. B.IFTEKHAR HUSSAIN, **B.KHALEELU REHMAN** "रोबोट से रोबोटटक्स तकः एक भारतीय पररप्रेक्ष्य" Scientific and Technical Terminology, Ministry of HRD, Govt. of India. March 2019.

5. Kalyan  Kasturi,D.Rajani,**B.Khaleelu  Rehman**,M.senthil  Kumar,K.Akhil,Uday,K.aravaind  "Low-cost,IOT-Based child safety Monitoring Robot with User-friendly mobile app"CISCON2021

6. **B.Khaleelu Rehman** , Sikendar alikhan,Kalyan Kasturi "Implementation of Electronics and communication Engineering Labs using virtual labs"A mini symposium on teaching learning practices by IUCEE,April 2022

7. Kalyan Kasturi,D.Rajani,**B.Khaleelu Rehman,**M.senthil Kumar "Online teaching method based on modified flipped classroom with debate and case study". A mini symposium on teaching learning practices by IUCEE, April 2022.

8. **B.Khaleelu Rehman,** G.Vallathan, Vetriveeran Rajamani, Mudasar Basha and Raman Kumar." Area Efficient High-Speed Binary Divider Using Xilinx IP Core" 3rd International Conference on Research in Sciences, Engineering & Technology (ICRSET-2022) at SUMATHI REDDY INSTITUTE OF TECHNOLOGY FOR WOMEN (Scopus indexed).

9. **B.Khaleelu Rehman**, G.Vallathan, Vetriveeran Rajamani, salauddin and Mudasar Basha "Implementation of 64 bit parallel subtract or using Xilinx IP cores for Fast Computing" 5Th International Conference on Intelligent Communication and Control Devices(ICICCD) at University of Petroleum & Energy Studies, Dehradun(( Scopus indexed) on 11th and 12th November 2022